A

Thesis

on

RADIATION HARDENED 14-T SRAM BitCell WITH OPTIMIZED POWER AND REDUCED AREA

Submitted in partial fulfilment of the

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Degree of

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in

VLSI Design

by

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May, 2020

DECLARATION

I declare that the work presented in this Thesis entitled " **Radiation Hardened 14 -T SRAM BitCell with Optimized Power and Reduced Area** ", submitted to the Department of Electronics and Communication Engineering, SEECE, Galgotias University, Greater Noida, for the Master of Technology in VLSI Design is our original work. I have not plagiarized unless cited or the same report has not submitted anywhere for the award of any other degree. I understand that any violation of the above will be cause for disciplinary action by the university against us as per the University rule.

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CERTIFICATE

This is to certify that the Thesis entitled **" Radiation Hardened 14 -T SRAM BitCell With Optimized Power and Reduced Area "** is the bonafide work carried out by Rajesh Kumar Raushan , during the academic year 2019-20. We approve this project for submission in partial fulfilment of the requirements for the award of the degree of Master of Technology in VLSI Design, SEECE, Galgotias University.

Dr. Mohammad Rashid Ansari
Project Supervisor

The Project is Satisfactory / Unsatisfactory.

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Internal Examiner (s) External Examiner

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ABSTRACT

The preference to optimize the performance metrics of overall performance, power, delay, leakage, and time to market (opportunity cost) has now not changed for the reason that progress of the IC enterprise. In truth, Moore's law is all about optimizing those parameters. however, as scaling of producing nodes progressed in the direction below 32-nm, some of the tool parameters couldn't be scaled any in addition, specifically the strength deliver voltage, the dominant component in figuring out dynamic electricity. This research is to lessen the power consumption, delay and higher efficiency in 12T and 14T SRAM cell for radiation hardened configuration and it is utilized in space applications. The backend device Synopsys HSPICE is selected for the analysis of power dissipation and delay of SRAM. In this work, 14T SRAM is designed and simulated in 22 nm era with the usage of FINFET technology. In proposed circuit 12t SRAM: Average power consumption is decreased by 99%, PDP is improved by 99.7%, EDP is decreased by 99%, propagation delay is improved by 79.2%. In proposed circuit 14t SRAM based improvements are: 99% in Average Power consumption, 76.5% in propagation Delay, 99.4% in PDP, 99.5% in EDP.

TABLE OF CONTENTS

Title	Page no
Acknowledgements	iv
Abstract	v
Table of Contents	vi
List of Figures	vii
List of Tables	viii
Glossary	ix
1. Introduction	
1.1. Introduction	1
1.1.1 Radiation Hardened Memory	5
1.2. Motivation	6
1.3. Problem Formulation	7
1.4. Research Problems and Objectives	7
1.5. Outline of the Thesis	8
2. Literature Survey	
2.1. Introduction	9
2.2. Survey of previous year papers	9
3. SRAM and FinFET Technology	
3.1. FinFET	14
3.2. Construction of a bulk silicon-based FinFET	15
3.2.1 Substrate	15
3.2.2 Fin etch	15
3.2.3 Oxide deposition	15
3.2.4 Planarization	16
3.2.5 Recess etch	16
3.2.6 Gate Oxide	17
3.2.7 Deposition of Gate	17

3.4 Challenges of manufacturing 18
3.5 FinFET versus Single-Gate Bulk MOSFET 19
3.6 FinFET Technology Development Guidelines 22
3.7 FinFET Based Digital Applications 22
3.8 SRAM 23
3.9 Existing Circuit for 14T SRAM Cell 24
4. IMPLEMENTATION AND RESULTS
4.1 Implementation of Proposed Circuit 27
4.2 Proposed Methodology 28
4.3 Results 29
5. CONCLUSION & FUTURE SCOPE
5.1 Conclusion 34
5.2 Future Scope 34

References 35
Appendices 38
FinFET Parameters and Model
The BSIM-CMG Model
List of Publications 43
1. Implementation of 12T and 14T SRAM bitcell using FinFET with optimized parameter.
2. An Assessment on SRAM using MOSFET and FinFET Technology in VLSI.

LIST OF FIGURES

Figure no **Page no**

Figure1.1 FinFET configuration (a) Independent Gate FinFET .
(b) Shorted Gate FinFET..(02)

Figure3.1 FinFET Device Schematics……..(22)

Figure3.2 FinFET Substrate……………………...(23)

Figure3.3 Fin etch & Oxide Deposition ………………..(23)

Figure 3.4 Planarization...(24)

Figure 3.5 Recess etch………………………...(21)

Figure 3.6 Silicon Based FinFET layer…………………………...............................(23)

Figure 3.7 The profile and Si loss of Si fins is controlled by careful wet clean,
Oxidation and etching ………………………………………………………(27)

Figure 3.8 Geometrical description of FinFET ....…………..……(28)

Figure 3.9 Drain-induced-barrier-lowering (DIBL) of a FinFET and a standard
single -gate bulk MOSFET for different gate lengths……………....................(29)

Figure 3.10 SRAM cell..(31)

Figure 3.11 CMOS based 12T and 14T SRAM bitcell........………………..…………...(33)

Figure 4.1 Proposed 12T SRAM Bitcell using FinFET 22nm ....…………………(34)

Figure 4.2 Proposed 14T SRAM Bilcell using FinFET 22nm..................……………..(35)

Figure 4.3 Average Power Comparison Result for SRAM Bitcell………………...……..(36)

Figure 4.4 Delay comparision Result for SRAM Bitcell…………………………………(37)

Figure 4.5 Average Power Comparison Result for SRAM Bitcell with Proposed
FinFET ……………………………………………………………………(37)

Figure 4.6 Delay comparision Result for SRAM Bitcell with Proposed
FinFET...(38)

Figure 4.7 EDP Result for SRAM Bitcell with Proposed FinFET ……………………...(38)

Figure 4.8 PDP Result for SRAM Bitcell with Proposed FinFET....…………………..…. (39)

Figure 4.9 MOSFET SRAM 14T Waveform..(40)

Figure 4.10 FinFET 14T Proposed Waveform for SRAM…… ....(40)

LIST OF TABLES

Table 3.1: FinFET Technology parameters

Table 3.2: Physical Models Used In Medici Simulations

Table 4.1: Simulation Output Results

GLOSSARY

RSP	Radiation hardened with speed and power
SRAM	Static ram
CMOS	Complementary metal oxide semiconductor
SOC	System -on-chip
VLSI	Very large-scale integration
SGFET	Shorted gates FET
IGFET	Independent gate FET
SNM	Static commotion edge
RHBD	Radiation hardened by design

Chapter 1

Introduction

1.1 Introduction:

Memory cells assume a critical job regarding force, speed and execution in computerized circuits, for example, the System_on_Chips (SoCs), microchips and microcontrollers. These type of memory clusters possess impressive piece of the chip region. Consequently, these memories. Cells as a general rule contribute for a higher division of the chip control. A few literary works have exhibited different designs for the SRAM cell, with their principle centre around decrease of the cell territory, diminished gadget include and decrease in the spillage control. The inclination to advance the design measurements of in general an ideal opportunity to advertise, costs, quality, territory, execution, has now not changed for the explanation that progress of the IC venture. In truth, Moore's law states about improving those requirements. in any case, as scaling of creating hubs advanced as underneath of 20-nm, a portion of the parameters in manufacture couldn't be scaled in any case moreover, explicitly the quality convey power, the predominant segment in making sense of dynamic power. This exploration is to diminish the utilization of intensity and off flows at the FINFET based SRAM cell. The backend recreation gadget Synopsys HSPICE is chosen for the examination of postponement and force scattering of SRAM. In this work, SRAM is structured at 22 nm time and furthermore and reenacted the use of FINFET innovation. Recreation result show that the current method offer improvement in term of postponement and force quality utilization over MOSFET.As nanometre technique technologies having innovative, running frequency and chip density have extended, making energy drainage in battery-operated hand held portable gadgets a first-rate concern. In any event, for no convenient gadgets, power utilization is basic in light of the improved bundling and cooling costs notwithstanding capacity unwavering quality issues. Along these lines, the rule configuration reason for VLSI (exceptionally enormous scope mix) creators is to meet generally speaking execution necessities inside a force financial plan. Scaling of door MOSFET in nm face remarkable task because of the extraordinary short channel impact that reason an exponential

development in the sub-limit and entryway – oxide spillage and DIBL. FINFET are encouraging substitute for bulk MOS at the nanoscale due to the fact the fabrication technology of FINFET and MOSFET almost identical Fin FET (fin-type DGFET) offer interesting strength –delay trade-off and higher characteristics (short channel effect) in nanometre which will meet the overall performance expected via the global technology roadmap for microelectronics for the drawing close technological node FinFET in ordered as a kind of hugeness metal oxide semiconductor field affect transistor/MOSFET. It turned out to be originally exceptional at the University of Berkley California by means of Chenning Hu and his associates. In FinFET the NMOSFET in CMOS structure innovation is supplanted with N-FinFET and PMOSFET with P-FinFET, at that point, the two entryways of FinFET are short aggregately. with the guide of the use of this methodology, we will design a FinFET model of a CMOS presence of mind circuit or a detour transistor decision making ability circuit that keeps similar functionalities on the grounds that the MOSFET model. Inside the period in the middle of, FinFET gives higher circuit exhibitions and lessens spillage present day by means of powerful concealment of fast channel impact and close best sub-edge swing. In the I-door mode, the quick channel results (limit voltage move off, sub edge swing debasement and channel provoked boundary decreasing) are really less extreme than those of the gadget inside the twofold entryway mode. Figure 1.1 shows two unique arrangements of. FinFET Device

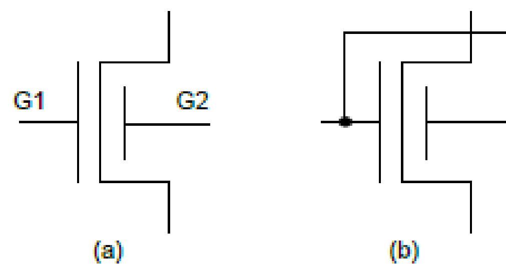

Figure 1.1: FinFET Configurations (a) Independent Gates (b) Shorted Gates

Extended transistor spillage as found in the lower development CMOS center points has in the end be an indispensable test in assessing the SRAM cells. The memory models utilizing trapezoidal heartbeat molded power nimbly are found to cause low power for the SRAM cell. These are called adiabatic SRAM cells and they commonly consider meet the basics of diminished power dispersal. The trapezoidal standard of the nimbly voltage draws in the charging and releasing of set aside power in the memory cell focus focuses and this partner in reducing the general power usage. Specific adiabatic method of reasoning sorts, for

example, the DCPAL, MCPL, 2N2P, 2N2N2P have been shown in the literature[2].Trapezoidal signs are used for adiabatic assignment and short out current reduction. The adiabatic essentialness dispersal of an adiabatic or the alleged imperativeness recuperation rationale circuit is less at lower frequencies, while it increments at higher degree of frequencies. This is in a general sense an immediate consequence of the lacking vitality recovery made at higher frequencies. This adiabatic justification standard can be recognizable in the SRAM cells with decrease the extent of force scattered in the circuits. In like manner, by looking at the particular SRAM cell structures, for example, the 4T, 5T, 6T, 7T, 8T and 9T contraptions (here, T shows the transistors), it has been indicated that the 7T structures depict improved make time edge also as unbelievable read static turmoil edge (SNM) without astounding enlargement in the chip area3. In this recommendation, an endeavor has been to look at the adiabatic memory cells utilizing CMOS and FinFET gadgets and existing FinFET circuits. The SRAM cells are looked at utilizing 6T, MCPL based 6T and transmission entryways based 6T structures and existing Circuits and the outcomes are broke down. The SRAM cells have been masterminded and repeated utilizing the FInFET gadgets too. The FinFET gadgets for these circuits have been picked considering the going with qualities: 1) The FinFETs are contained very little and undoped body, which helps in covering any spillage ways for current stream in the contraption, and in this way in diminishing SCEs (Short Channel Effects) of the gadgets. 2) Because of the painstakingly doped body, the limit voltage is controllable.while it increments at higher degree of frequencies. This is on a very basic level an immediate consequence of the inadequate centrality recovery made at higher frequencies. This adiabatic method of reasoning standard can be recognizable in the SRAM cells with diminish the extent of force disseminated in the circuits. In like manner, by looking at the particular SRAM cell structures, for example, the 4T, 5T, 6T, 7T, 8T and 9T contraptions (here, T shows the transistors), it has been indicated that the 7T structures depict improved make time edge correspondingly as mind blowing read static commotion edge (SNM) without stunning growth in the chip area3. In this recommendation, an endeavor has been to look at the adiabatic memory cells utilizing CMOS and FinFET gadgets and existing FinFET circuits. The SRAM cells are looked at utilizing 6T, MCPL based 6T and transmission entryways based 6T structures and existing Circuits and the outcomes are broke down. The SRAM cells have been masterminded and imitated utilizing the FInFET gadgets too. The FinFET gadgets for these circuits have been picked considering the going with qualities: 1) The FinFETs are contained amazingly little and undoped body, which helps in covering any spillage ways for current stream in the

contraption, and in this way in diminishing SCEs (Short Channel Effects) of the gadgets. 2) Because of the painstakingly doped body, the limit voltage is controllable.

The yearning to smooth out the masterminding estimations of execution, power, district, cost, and time to publicize (opportunity cost) has not changed since the beginning stage of the IC trade. In all honesty, Moore's Law is all concerning improving those parameters. In any case, as scaling of making center points progressed towards 20-nm, a portion of the device parameters couldn't be scaled to any degree further, particularly the limit give voltage, the predominant think about basic extraordinary force. In addition, most typically improving for one factor like execution exactly changed over into gigantic exchange offs in elective zones, like force Another hindrance as methods advanced toward 20-nm was the very conviction that lithography was face an issue at ArF lighting up flexibly with a frequency of 193nm however the strategy essential component was pushing sub-20nm. Optical advancements like dousing lithography and twofold atterning made that possible, in any case at cost of raised variability. There have been moreover elective improvements in transit like high-K metal door that relieved
– partially – entryway spillage. In any case the very reality remained that as the structure window for smoothing out among a comparable arrangement factors was contracting. masterminding in FinFET grows the organizing window once more. in movement voltage continues scaling down, amazingly getting a good deal on one of a kind and static force. Short channel impacts are diminished broadly, and decreasing the watchman banding expected to administer change. Besides, execution continues improving appeared differently in relation to planar at a regulated center. Honestly, at dreadfully low force give voltages, the execution favored viewpoint of the FinFET appeared differently in relation to its planar equivalent stretches out taking into account the common door the administrators of the channel inside the FinFET. For memory originators, an extra good situation of FinFETs is that the stunningly lower support voltage needs of FinFET-based SRAMs appeared differently in relation to planar FETs. Given the rising estimation of execution per unit power (Koomey's Law), one important style upgrading bit of leeway of FinFET appeared differently in relation to plan is way more performance at a proportionate force expenditure plan, or equal performance at a far lower power spending plan. This essentially enables originators to remove the best execution for disgraceful force, a pressing improvement for fuelled contraptions. One component that makes the advancement from considering with planar FETs to devising with FinFETs to some degree less befuddled is

that the showed fact that the back-finish of the methodology is basically a corresponding, subsequently a bit of the masterminding stream connected to the physical execution remains perfect.

VLSI, is a sort of technique this way to frame incorporated circuits by joining a great many devices into one IC. The microchip could be a VLSI gadget. Every single each chip production line made nowadays use VLSI models. Current development has bounced from the improvement of bigger devices on single IC to a micro-chip with a couple of entrances with millions of individual transistors of minimal dimensions. For the reason that of this modified course of action it finds scope inside the fields of tip top enlisting and correspondence structures, objective frameworks, wafer-scale mix, equipment systems and assessment and improvement. Thusly there's a rising enthusiasm for the chip determined things inside the present and future. To satisfy with these solicitations we will in general should diminish the scale, force, and quality. Out of that power dispersal has turned into a pivotal goal inside the style of every simple and advanced circuits. it's shown that gratitude to ignoring short out current, past systems intended to advance the domain of a fan-out tree could prompt over the top power consumption.

The data of the FinFET circuit configuration is normally given after observed the writing audit. There are numerous sort of criteria and different kind of advancement the FinFET circuit dependent on the analyst's and perspective that they take. To guarantee the criteria and angle for any FinFET, as per the writing audit here must be directed that can be investigated after. Fundamental point which are identified with the FinFET just are audit in this part.

Presently days FinFET become an alternate gadget for the nanoscale plan yet FinFET might be another gadget structure of vertical twofold gate. FinFET is dependably a piece of test of MOSFET on the basis that it have a special property. This tool has the electrical coupling between the back side and the front side mos transistor. It offers imaginative ckt arrangement styles because of its two fold gate structure. FinFET makes very rapid sending to assembling as the building of FinFET is perfect with customary CMOS [1].

FinFETs are quasiplanar field-impact transistors. The gadget material science overseeing the usefulness of FinFETs is actually equivalent to that of planar MOSFETs. A silicon film of thickness TSI is structured on a SOI wafer. The gate folds around the opposite sides of the blade. The channel is framed reverse to the level of the wafer. Its length is showed up as LG. This is the reason that the gadget is named quasiplanar. The viable size of FinFET is 2nHFin, n denotes the quantity of balances and HFin define the balance

stature. Thusly, increasingly broad transistors with higher on-stream are made possible by using various blades. Fig. 1.5 shows, construction for FinFET using two balances. It should be seen that FinFET width is quantized, similar to the amount of balances. This prompts basic diagram thoughts, for instance, helpfulness, execution and power, which are fragile to the extent.

FinFET tool are advanced by a dainty silicon_body. The thinness is call Tsi are wrapped by gate terminals. The channel is enclosed opposite to the level of the wafer and the induced current streams similar to the wafer plane [2]. By drawing the gate anode at the highest to the channel, the FinFET proficient the sovereign control of the back end and the front gates.

1.1.1 Radiation Hardened Memory:

Consistent increase in transistor, combined along with developing interest for small voltage, small power applications, expands the weakness of VLSI chip to delicate errors, particularly when presented to extraordinary ecological conditions, for example, those experienced by space applications. The large amount of power of these circuits are consumed by memory that spread enormous territories of the Si bite the dust and regularly save basic information. Radiation solidifying of inserted memory squares is normally accomplished by actualizing amazingly enormous bit-cells or excess exhibits, keeping up a generally large working voltage; be that as it may, notwithstanding the subsequent region overhead, this regularly restrains the base working voltage of the whole framework prompting noteworthy force utilization. SRAM plan for small voltage activity has gotten progressively well known in the ongoing past. Different bitcell structures and engineering strategies have been existing to empower activity profound in subthreshold locale [15], [18, 19, 20,21].These plans commonly include the expansion of various transistors into the bit-cell structure, contrasted and the benchmark 6T SRAM bit cell, exchanging off thickness with vigorous, low-voltage usefulness. Notwithstanding, these bitcells ought to be intended for activity under standard working situations, and in this manner, don't give adequate strength to SEUs beneath high-radiation situations. What's more, the plan engineering of these phones depends on the typical 6T cell; in this way, the 6T cell has a similar solidifying capacity to most, if not all, these unprotected cells.

Delicate errors or single-occasion upsets (SEUs) brought about by radiation attacks is the essential drivers of disappointment in VLSI circuits working inside a profoundly transmitting

condition. In like manner, keeping up information uprightness considering SEUs has become an indispensable part of memory cell plan [4]. Delicate errors happen when a vigorous molecule hits and goes through a semiconductor element, possibly causing somewhat change in the memory cell [5-6]. At the point when the molecule hits a turn around one-sided p-n-intersection, for example, a transistor dissemination mass intersection, the infused charge is moved by float and causes a momentary current heartbeat that changes the hub voltage. Information misfortune happens when the gathered charge (Qcoll) surpasses the basic charge (Qcrit)that is put away in the touchy hub. The charge stored by a molecule strike can be determined from the necessary of the transient current heartbeat, and Qcritis characterized as the base charge kept in a delicate hub that outcomes in a memory bit change [7].

1.2 Motivation:

Forceful Scale down the components of MOSFETs is typically a nonstop design. At the point when we attempt to decrease size of MOSFET the principle troubles are occure with the semiconductor device creation process, the prerequisite for amazingly low voltages, and with progressively sad electrical execution the need of circuit modify and improvement [2]. It has been communicated that more diminutive transistors filled in as switch speedier, which is the major motivation for cutting back the components of semiconductor contraptions [2].As consistent scaling of CMOS innovation, the base separating between the transistors is diminished. Along these lines, to various transistors are inclined to the charge set from a singular atom hit appear differently in relation to progressively prepared procedures where only one mos_transistor was impacted [2]. The induced charge allotment results in single_event with multiple_node upsets (SEMNU), which is the effect of dynamic part strikes in nanometre CMOS advancement [3], [4]. Likewise notwithstanding, flexibly voltage ceaselessly decline results expands the flimsiness of circuits to radiation. Along these lines, the advancement of solidified because of radiation innovations in computerized circuits is exceptionally dire [5]. As a result of the more vital fragile volume per bit and capacitance at lower center point than the dynamic accomplice, SRAM is progressively disposed to soft_error. In this manner, the delicateerror annoyed (SER) [6] in SRAM is extended with the development scaled in the nm framework. For decreasing the SER, different substitutes are existing by researchers to the conventional 6T SRAM cell [7-15]. The standard fortification technique is through making specific structure of transistor sifts through cells to accomplish c-levehipl insurance.

1.3 Problem Formulation:

SRAMs keep on possessing a ruling bit of the all-out territory and power in present day ICs, the subsequent absolute power funds are critical. Lamentably, be that as it may, regular SRAMs, in light of the 6T bit-cell, neglect to work at Low voltages, on account of diminished flag levels and as a result of expanded variety. To address these confinements, a 8T bit-cell is fused, it accomplishes full read and write usefulness. The benefit of diminished power consumption of the current 8T cell engages it to be used for battery worked SoC structure. Future and utilizations of the existing 8T cell can conceivably be in low/ULV and medium recurrence activity like neural flag processor, sub limit processor, wide-working extent IA32 processor, quick Fourier change center, and low voltage store task.

Voltage scaling is a successful procedure for limiting the power consumption of SRAMs. Further, as SRAMs keep on involving a commanding segment of the absolute zone and power in present day ICs, the subsequent all out power funds are huge. Shockingly, in any case, traditional SRAMs, in light of the 6T bit-cell, neglect to work at Low voltages, in view of decreased flag levels and as a result of expanded variety, to address these constraints, a 8T bit- cell is joined, it accomplishes full read and write usefulness. The upside of diminished power consumption of the existing 9T cell empowers it to be utilized for battery worked SoC plan.

1.4 Objective:

The main objectives of this thesis are:

- To do research and literature review of SRAM based circuits.
- To study radiation hardening effect on SRAM cells
- To study logic on 14 SRAM cells for space applications
- To simulate a new design on HSPICE and compare results with the conventional circuits using FinFET technology.
- The results to be compared with Average Power Consumption, Delay, Power Dissipation and Energy.

1.5 Outline :

Following chapters are there in the thesis:

Chapter 1 consists of introduction and need of SRAM cell in space application and radiation hardened memories.

Chapter 2 consists of literature review of previous papers related to SRAM.

Chapter 3 gives explanation of 14T SRAM and FinFET Technology.

Chapter 2

Literature Review

2.1 Introduction:

This chapter, a complete literature review is given on the basis of study of previous papers. About 28 paper are reviewed and analysed related to SRAM in different transistor count circuits.

2.2 Survey of previous year papers:

[1] Chunyu Peng et. al., In this reference article, a new radiation-solidified 14-transistor SRAM bitcell with power, speed propelled radiation-toughened by power speed improved [(RSP)- 14T] for application in space design was proposed. By circuit-and configuration level improvement structure in a 65nm CMOS advancement, the 3-D Technology_CAD (TCAD) mixed mode amusement results show that the construction is invigorated extended to single-event steamed similarly as single-event different center point upsets due to the sharing of charge between a kind of transistors which is off. Furthermore, the HSPICE reenacted results explains power usage and compose speed of the creator proposed RSP-14T and results are amended by _66% and _55%, exclusively, differentiated and that of the radiation solidified arrangement (RHD)- 12Transistor memory bit_cell.

[2] Jaeyoung Kim et. al., Near-threshold activity is accumulating developing consideration for ultra-low force applications in spite of the reality the unwavering quality of the close threshold advanced frameworks warrants uncommon examination of strength measures to guarantee right usefulness under stringent ecological and producing dispersing particulars. In this reference paper, a perfect hypothetical write & read static commotion edges (RSNM/WSNM) is talked about. Likewise, a 12Transistor SRAM bitcell is author planned so as to come to the hypothetical WSNM limit. This might be accomplished by taking out a criticism of consecutive inverters by methods for information subordinate stockpile detach in write activity. This permits the author wished-for bit cell to develop write edge significantly. Numerous past works likewise endeavor to cutoff the stock, however a large number of them could not information subordinate. Monte-Carlo (MC) recreation outcomes show the author wished-for 12Transistor SRAM bitcell is dynamically

overwhelming in static and dynamic disturbance edge than the conventional 6Transistor and 8Transistor SRAM bit cells similarly as a 10Transistor piece cell.The territory overhead of the author proposed bit cell is 1.96 occasions and 1.74 occasions more prominent than the 6Transistor and 8Transistor bit cells, individually. Scientific models of WSNM for the 12Transistor piece cell in the super-threshold locale and the sub-threshold area are likewise author planned.

[3] Asifa Amin et. al., With on developing innovation scaling, low force activity has gotten significant in VLSI plan. SRAM comprises huge bit of the advanced VLSI plans, along these lines endeavors are being made to configuration low power SRAM utilizing various ways. This reference paper talks about different author proposed SRAM plans, comprising of various number of transistors from each other. This reference paper centers around the investigation of these plans and their examination based on parameters like force scattering, access time, dependability and force postpone item. All the SRAM structures has diverse read write activity and subsequently various outcomes. It was discovered that 12T SRAM has better execution if there should be an occurrence of intensity scattering and force postpone item however high access time than the other author proposed SRAM cells when thought about based on reproduction results acquired on 45nm condition utilizing Microwind instrument.

[6] Chien-Cheng Yu et. al., In this reference paper, another single_port five_transistor (5T) SRAM cell with integrated read & write help is author proposed. Among the help hardware, a voltage control unit circuitary is coupled to the sources comparing to driver circuitry of each column memory bitcells. This setup is expected to control the source voltages of acess transistors under various working modes. In particular, during a write activity, by methods for measuring the driver transistor near bitline to determine the write '1' issue. Also, related with a two-organize reading system to speed up and to keep away from superfluous force utilization. At long last, with the backup fire up circuit structure, the cell can change to the reserve mode rapidly, in this manner diminish leakage current in reserve.

[8] Jyoti Verma et. al., This reference paper talk about planning of low force, rapid 10Transistor (10T) StaticRAM and investigation of StaticRAM cell in MetalOxideSemiconductor Field Effect type Transistor (MOSFET) and FinFET innovation.

MOSFET is utilized broadly in numerous regions, however beneath 40 nm innovation control of channel area turns out to be very upsetting. Accordingly, there is a need for new inventive innovation which permits originators to plan beneath 40nm innovation and can offer great power over gate in this way diminishing short channel impacts. The planning of StaticRAM is examined utilizing TANNER EDA instrument and Microwind.

[9] Lior Atias et. al., Continuous scaling of transistor, combined with the developing interest for less potential , less-power applications, builds the powerlessness of VLSI designed circuits to delicate faults, particularly when presented to outrageous natural surroundings, for example, those experienced by space applications. The furthermost powerless of these device are memory clusters that spread enormous regions of the material silicon bite the dust and regularly store basic information. Radiation solidifying of implanted memory squares is ordinarily accomplished by actualizing incredibly huge bitcells or excess clusters and keeping up a generally high working voltage; be that as it may, notwithstanding the subsequent region overhead, this regularly constrains the base working voltage of the whole context prompting critical force utilization. In this reference paper, author propose the primary radiation-hardened SRAM_ bitcell focused at reduced-voltage usefulness, while keeping up high delicate error heartiness.

[10] B.K.Kaushik et. al., This reference paper manages the structure chances of StaticRam (SRAM) for reduced power Feasting and engendering postponement. Author have examined both read edge for read capacity and write edge for SRAM write capacity. Static Noise Margin influences both read edge and write edge. Author have broke down the NoiseMargin (Static) utilizing customary butterfly strategy which requires the revolution of VTC by 46 degrees. SRAM cell is broke down concluded the in view of of various sort of examination.

[13] Biswarup Pal et. al., SRAM cell (StaticRAM) is a memory used to store information. Reduced-Power and High-Concert have turn out to be a consuming issue in VLSI enterprises nowadays. Among the different installed memory advances, SRAM can give the best while keeping up low backup power utilization. High seepage current in profound submicron innovation is turning into a critical supporter of the force dissemination of CMOS circuits as the device threshold voltage, gate oxide thickness and length of channel are decreased.

Because of extreme scaling of CMOS gadget, low force is the significant test for the present hardware enterprises. In the course of most current couple of decades, author are downsizing the CMOS gadgets to accomplish better execution as far as speed, power dispersal, size, and unwavering quality.

[15] Ujwal Shirode et. al., Author examine Schmitt-Trigger (ST) based disparity detecting StaticRAM (SRAM) bit_cells for verylow voltage activity. The ST-based StaticRAM bit_cells report the key clashing plan prerequisite of the read versus write activity of an ordinary 6Transistor bit_cell. The ST activity gives better read-dependability just as better read-disappointment likelihood contrasted with the standard 6Transistor bitcell. The author planned ST based bitcells incorporate an implicit criticism system. Adjusting the exchange offs between little zones, little powers, quick writes & read are a fundamental piece of any StaticRAM structure. That is, StaticRAM formation requires adjusting among different plan criteria, for example, limiting cell region utilizing littler transistor, looking after writes & read soundness, limiting force utilization by decreasing force supply, limiting read/write entree time, limiting drip current, diminishing piece line thump to lessen power utilization. A nitty gritty examination of 6Transistor bitcell shows that the ST created bitcell can run at reduced potential.

[16] S.Munaf et. al., Memories are the significant piece of any computerized framework and no advanced framework can be finished without recollections. Smaller gadgets and installed frameworks are developing, so the low force utilization is fundamental to the structural framework plan .Optimization of the force at the coherent level is one of the most significant assignment to limit the force. With expanding innovation, use of SRAM Cells has been expanded in huge degree while planning the framework on-contributes CMOS innovation, this audit article is likewise founded on that. In this article centers around the examination in wording extraordinary kinds of SRAM are structured so as to fulfill low force, elite, deferral and territory.

[17] Rukkumani V et. al., Normally charge reusing (CR) rationale is utilized to lessen power in SRAM memory cells.The read admittance time of 8T SRAM cell is marginally debased in read as "0" activity. At the point when the bit_cell is in zero express, the bitline release along BT takes longer because of lower conductance of N type MOS transistor.Two 4by4 SRAM macros have been actualized in a standard 180 nm CMOS process utilizing the

8Transistor and the 10Transistor cells. The two macros have indistinguishable location translators, information line drivers and sense intensifier structure. Broad Read/Write tasks have been mimicked at 27,50,75 and 100° C to evaluate the exhibition of the author future plan. Every one of the circuits recreations are planned with 250 MHz and 300 MHz working recurrence with source voltage of 3.3 mV. It is obvious that at both working frequencies, the author proposed 10Trasistor SRAM configuration has altogether less read force utilization. This is on the grounds that just a single cell is turned on rather than every one of the cells in a single column in the ordinary structure. The static and dynamic force likewise determined for the two SRAM plan with different temperature ranges.

Chapter 3

SRAM and FinFET Technology

3.1 FinFET:

FinFET, otherwise called Fin type Field Effect Transistor, is a rather "3D" or non-planar transistor utilized in the structure of current processors. As in prior, planar structures, it is based on a SOI (silicon on encasing) substrate. In any case, FinFET plans likewise utilize a directing channel that ascents over the dimension of the protector, making a dainty silicon structure, molded like a balance, which is known as a gate cathode. This balance molded anode enables various gates to work on a solitary transistor.

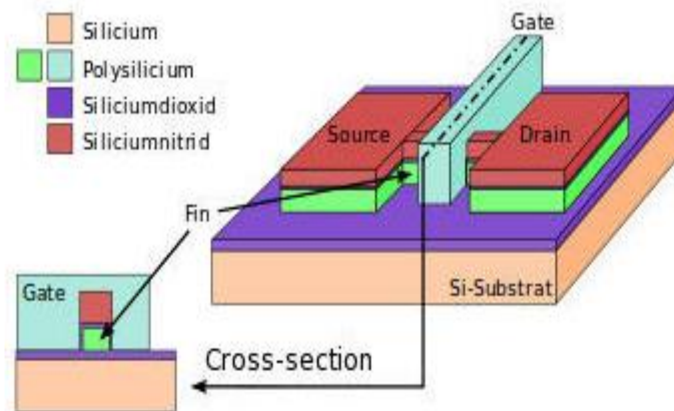

Figure 3.1: FinFET Device schematic

CMOS contraptions cause high spillage current, extended sub-limit spillage and consolidate parasitic type capacitances. These can be overwhelmed by the contraption FinFET. As appeared in Figure 3.1, the primary Gradual_channel of the FinFET gadget is enveloped by a modest silicon edge. This is the key part of FinFET on or after the mass CMOS gadget associates. The noteworthy channel length of the FET is contrasting with the sharp edge thickness. This adjustment covering reduces the spillage by enlightening the electrical authority over gradual_channel. Likewise, the FinFETs give healthier governor over the short gradual_channel impacts, when stood apart from CMOS. That lessened spillage current vintages diminished energy usage in the contraption. Thusly, the FinFET goes about as a little power solid contraption and the FinFET gadget ends up being a

productive decision for the massive CMOS transistors. FinFETs are utilized in various game plans, to be express , the 'Twofold Gate' (DG) strategy where together the doors are shorted to perceive speedier exchanging of for FinFET gadget, and 'Back Gate' (BG) mode5 in which the two gateways stay secluded.

3.2 Construction of a bulk silicon-based FinFET:

3.2.1 Substrate:

Reason for a FinFET is a delicately p-type semiconductor doped substrate with a hard cover on top (for example silicon nitride) just as a designed oppose layer.

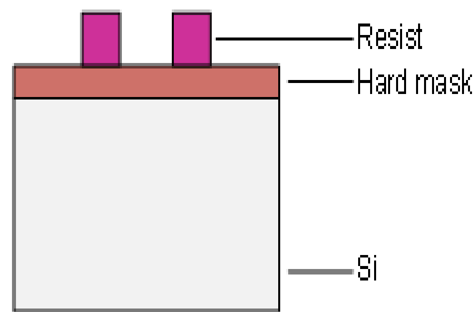

Figure 3.2: Substrate

3.2.2 Fin etch:

The blades are shaped in an exceptionally anisotropic engraving process. Since there is no stop layer on a mass wafer for what it's worth in SOI, the engraving procedure must be based on time. In a 22 nm procedure the width of the balances may be 11 to 16 nm, the tallness would in a perfect world be twice that or more.

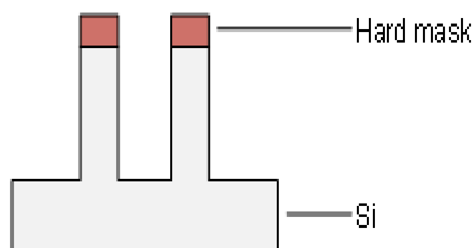

Figure 3.3: Fin etch

3.2.3 Oxide deposition:

To separate the balances from one another , an oxide testimony with a high point of view extent filling conduct is required.

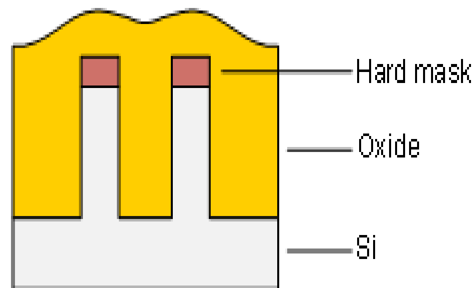

Figure 3.3: Oxide deposition

3.2.4 Planarization:

The oxide is done planarized by compound mechanical cleaning. The hard cover goes about as to stop layer.

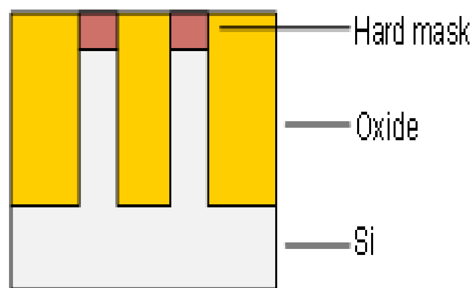

Figure 3.4: Planarization

3.2.5 Recess etch:

Another engraving procedure is expected to break the film of oxide to shape a sidelong detachment of the balances.

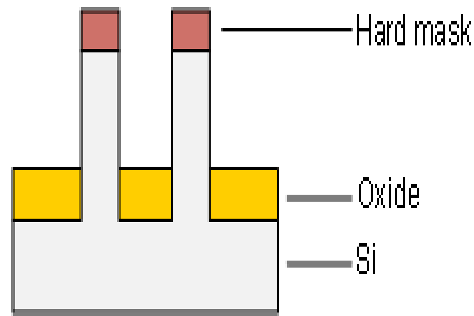

Figure 3.5: Recess etch

3.2.6 Gate Oxide:

Over the balances the gate oxide is kept by means of warm oxidation to separate the gate terminal from the channel. Because the blades are as yet associated beneath the oxide, a high-portion calculated embed at the basis of the balance makes a dopant intersection and finishes the detachment (not outlined).

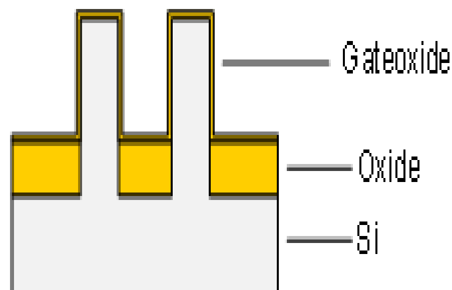

Figure 3.5: Gate Oxide

3.2.7 Deposition of Gate :

At last, an exceedingly n+-doped silicon layer of poly is kept over the blades, in this manner up to three gates are folded over the channel: one on each side of the balance, and - relying upon the gate oxide on top the thickness of a third gate above.

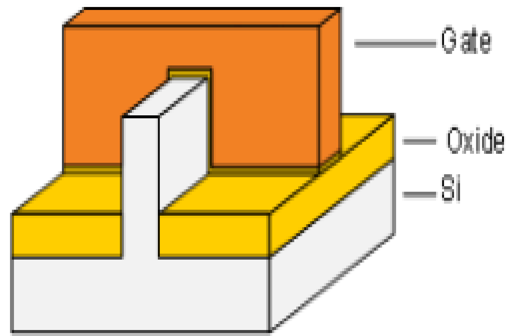

Figure 3.6: Deposition of Gate

The impact of the topmost gate can likewise be hindered by the testimony of a nitride layer over the channel.

As there is a layer of oxide on a SOI wafer, the channels are confined from one another at any rate. Moreover the engraving procedure of the blades is disentangled as the procedure can be halted on the oxide effectively.

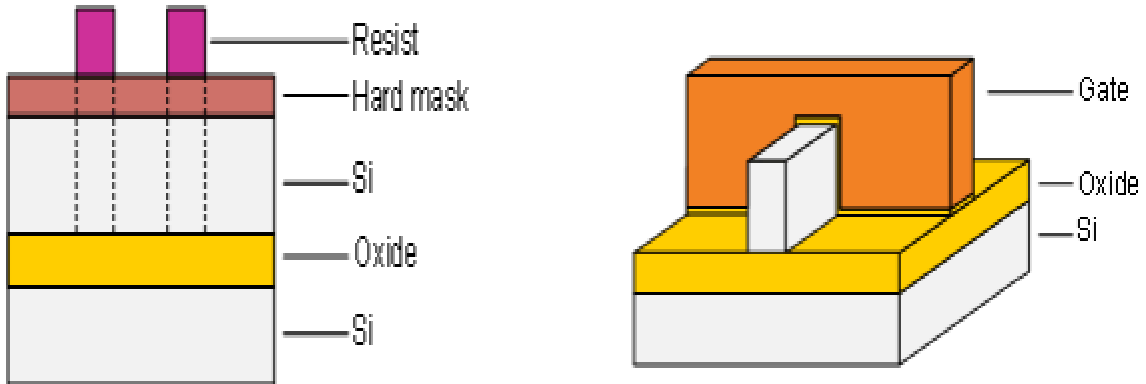

Figure 3.6: silicon-based FinFET Layer

3.4 Challenges of manufacturing:

What's more, a couple of new procedure, gadget, and type of materials encounters in assembling 10 to 22nm FinFET are condensed beneath.

Directly from the beginning, the Si surface on balances appears to be more defenseless than in mass. The profile of Si adjusts is compelled through mindful wet clean, oxidation,

implantation, and scraping the low-doping of equalization and vertical dopant profile control can restrict Vt assortments of transistors.

Additionally, the strong source (PSG or BSG) sub-balance doping is persuading to cover punch-through spillage current. So as to divert dopant spread upward into the dynamic equality channel from the sub-balance doping an area, the mass FinFET can be framed with species (for example C, F, N) got along with strong dopant hotspot for covering dopant dispersing. On the other hand, a nearby oxidation structure can achieve oxide underneath (balances on-oxide) for amazing constrainment by the base oxidation-through-STI (BOTS) framework. The penetrable STI oxide fills in as a catch to hold the leveling from slanting amidst front line base oxidization.

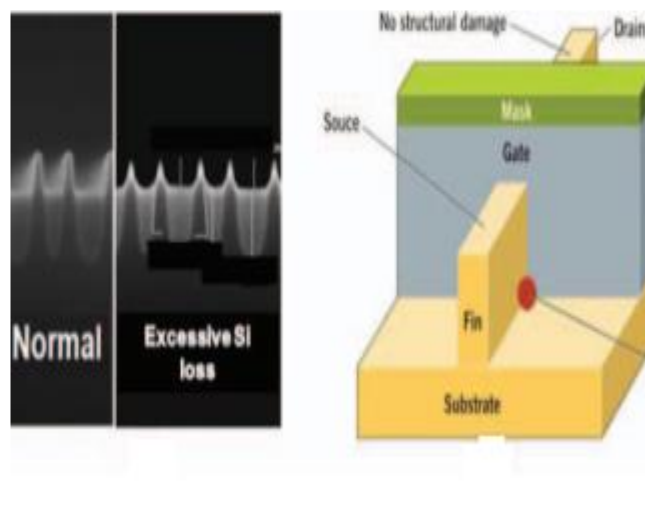

Figure 3.7: The profile and Si loss of Si fins is controlled by careful wet clean, oxidation, and etching

Thirdly, the diminished condition of sharp edges can provoke progressively expansive Vt spread, yet it is conceivably fixed by vertical embed of N2 (for changing close by WF) . Correspondingly, a multi-Vt plot for SOC can be acknowledged by utilizing different segment of decreased front lines with vertical addition dopants (N, Al, C, and so on.) into WF layers (for changing WF) rather than executing the over the top diverse work-work (WF) and really ruining yield amidst entryway stack strategy.

3.5 FinFET vs Single Gate Bulk MOSFET:

The FinFET and the single-door mass MOSFET progresses are considered in this section for short-channel impacts. The limitations of the FinFETs estimated in this part are recorded

in Table beneath. The mass MOSFET is arranged with entryway length = 31nm, door channel/source spread = 3.2nm, transistor width = 31nm, entryway oxide thickness = 1nm,, a polysilicon gate with doping fixation = 4x1021 cm-3, and a great corona doped channel. The varieties of the edge voltage (Vth) and the drain-prompted hindrance bringing down (DIBL) with the gate dimension are portrayed in individuallyThe plan contemplations are done based on the geometry depiction of FinFET gadget structure. Fig.3.1 demonstrates the geometry portrayal of FinFET.

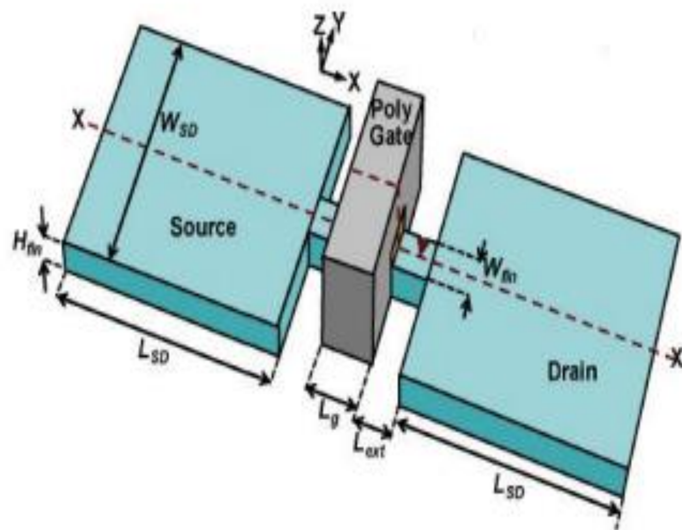

Figure 3.8: Geometrical Description of FinFET

Table 3.1: FinFET Technology parameters

Parameter	Value
Gate length (L)	32 nm
Gate-Drain (Source) overlap	3.2 nm
Fin Height (H_{fin})	32 nm
Fin thickness (t_{si})	8 nm
Oxide thickness (t_{ox})	1.6 nm
Channel doping	10^{15} cm^{-3}
Source / Drain doping	2 x 10^{20} cm^{-3}
Work function (N-FinFET)	4.5eV
Work function (P-FinFET)	4.9eV
Supply voltage (V_{DD})	0.8V

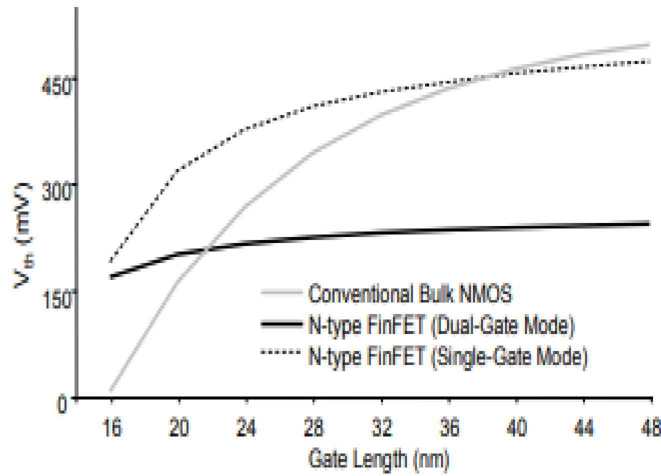

Figure 3.8: The variation of the V_{th} with the gate length for a FinFET and a standard single-gate bulk MOSFET.

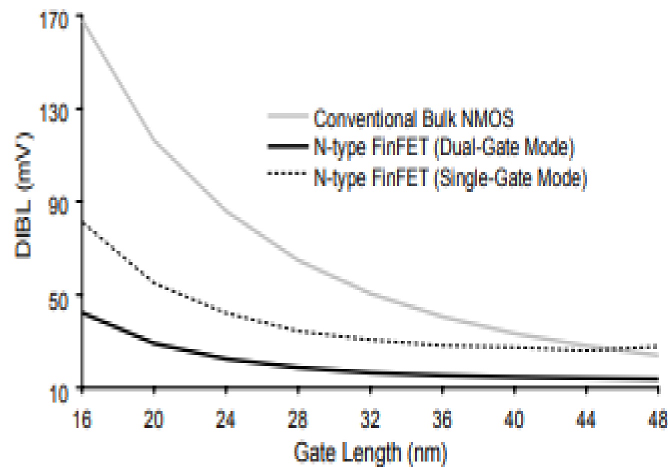

Figure 3.9: Drain-induced-barrier-lowering (DIBL) of a FinFET and a standard single-gate bulk MOSFET variation with gate lengths.

The constraint of voltage at the source-to-gate potential changes current at drain terminal per balance stature is 10-5 A/µm for |VDS| = VDD. DIBL is estimated as the debasement in |Vth| when the voltage at drain is expanded from 0.05V to VDD. The short-channel impact (Vth-move off) is altogether smothered with the twofold gate FinFET. The reliance of the edge voltage on the gate length is a lot more fragile for a twofold gate FinFET when contrasted with a solitary gate mass MOSFET. Moreover, the DIBL saw with a twofold gate FinFET is fundamentally littler when contrasted with a solitary gate MOSFET.

3.6 FinFET Technology Growth Strategies:

In this area, FinFETs with various blade depth and gate oxide depth are planned and portrayed for DC qualities, spread postponement, and constraint varieties affectability on the 32nm hub. The length of gate, the gate-drain or source covers, and the blade tallness are fixed at 31nm, 3.1nm, and 33nm, separately, for every one of the appliances considered in this Section. The balance thickness is fluctuated from 8nm to 20nm. For each balance thickness the gate oxide thickness is changed from 1.1nm to 2nm. Twenty unmistakable gadget setups with various mixes of balance thinness and gate oxide thickness are well-thought-out in this paper. For every gadget setup, the gate work-work is picked to such an extent that the limit potential is equivalent to 308mV and - 408mV for the N-FinType and the P-Fin type transistors, individually, while working with a 0.7V supply voltage (VDD = 0.7V). The device physical models joined in every one of the recreations achieved in this area are recorded in a Table 3.2. The impact of the procedure constraint varieties, the supply potential varieties, and the temperature of vacillations on the qualities of FinFET gadgets.

Table 3.2: Physical device Models Used In Medici Simulations

Physical Model	Description
QM.PHILI	Accounts for quantum mechanical effects in the inversion layer
CCSMOB	Accounts for carrier-carrier scattering, lattice scattering, ionized impurity scattering, and temperature
SRFMOB2	Accounts for surface scattering with surface roughness, phonon scattering, and charged impurity scattering considered
FLDMOB	Accounts for the dependency of the mobility on the parallel electric field

3.7 FinFET Based Digital Applications:

Cmos Inverter, NAND and NOR entryways are essential part in any contraption circuits. According to International_Technology_Roadmap for Semiconductors (ITRS), in current world's circumstance 93.99% of chip zone is included by memory where trading

exercises are finished by the circuits different M times. This demands the circuits to work in fast and besides power employments of introduced memory of computerized circuits to be diminished. Cutting down the gracefully potential is extremely fruitful in power saving anyway scaling down the flexibly of intensity using standard MOS_FET having an issue due to SCE. Along these lines, FinFET might be used as a decision to quantify power flexibly at decreased leval.

3.8 SRAM:

Static kind of arbitrary access memory (static RAM or SRAM) is a kind of semi_conductor memory that abuses bistable locking hardware (as like flip-flop) to store each piece. StaticRAM shows data remanence anyway it is so far flimsy in the conventional rationale when the memory isn't controlled that information will be lost. The term static isolates StaticRAM from DynamicRAM (dynamic arbitrary access memory) whiich must be irregularly stimulated. SRAM is quicker and more exorbitant than DRAM; it is routinely utilized for CPU reserve or information store while DRAM is worked for a PC's crucial memory. The principal memory circuit is concocted to be static if the data of stored on it can be held uncertainly, as long as the force flexibly is available, with no prerequisite for irregular animate action. The data accumulating cell, i.e., the one-piece memory cell in the static RAM displays, unendingly contains an essential snare circuit with two stable working core interests. Dependent upon the shielded state of the two inverter lock circuit, the information being held in the memory cell will be deciphered either as rationale '0' or as rationale '1'. To get to the data bound in the memory bitcell by methods for a bitline, we need atleast one switch, which is compelled by the looking at word line as showed up in Figure 3.11.

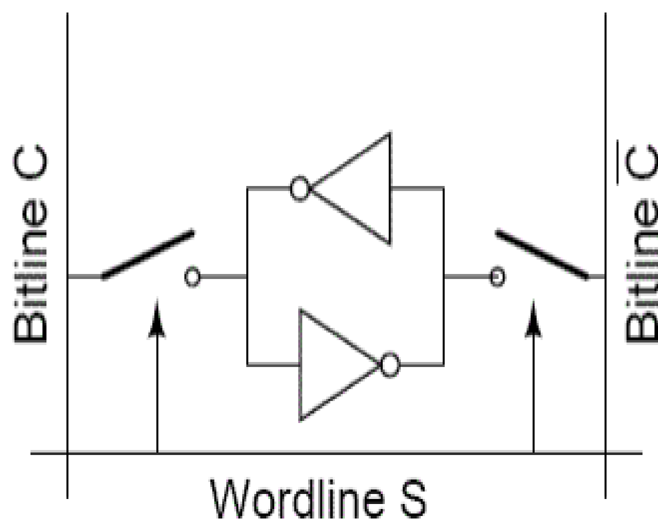

Figure 3.10: SRAM cell

Static random access memories (SRAM) can hold its stored data insofar as power is provided. This is rather than dynamic RAM (DRAM) where intermittent revives are fundamental or non-unpredictable memory where no force ought to be accommodated data upkeep, as gleam memory. The term "random access" implies that in a variety of SRAM cells every cell can be read or written in any request, irrespective of which cell was last gotten to. The structure of a 6 transistor of SRAM cell, putting away one piece of data. The heart of the cell is construct by two cross coupled CMOS inverters, where the yield capacity of every inverter Vout is continued as impact to the following .Vin This information hover adjust the inverters to their different state. The appearance transistors and the word line and bit lines, WL and BL, are used to peruse and compose from or to the cell. In reinforcement mode the word line is low, executing the section transistors. In this express the inverters are in correlative state. Right when the p-type channel MOSFET of the left inverter is turned on, the potential Vl ,out is high and the p-type channel MOSFET of inverter two is slaughtered, is Vl ,out low. To write data the information is forced on the bit line and the backwards information on the opposite piece line. At that point the entrance transistors are turned on by setting the word line to high. As the driver of the bit lines is a lot more grounded it can state the inverter transistors. When the data is gathered in the inverters, the entry transistors may be killed and the data in the inverter is protected. For reading the word line is swung on to initiate the entrance transistors although the data is detected at the bit lines.

3.9 Existing Circuit for 14T SRAM Cell:

Contrasted and RHBD-12T, the radiation hardness was upgraded by the stronghold of tedious center points also additional two new pMOS transistors. In addition, on account of the store of the division where the dreary center points discovered are compelled by the extra new PMOSs, throughout the time of write activity, the input component will be hindered effectively. Hence, the write speed and force utilization have been upgraded viably. By and large, Zest proliferations by using the twofold exponential current cause model are applied for evaluating the radiation flexibility of the gadget circuit, which is proficient. Regardless, the model relies upon arrangement imperatives that are not physical [16].

The schematic plan of the proposed RHBD-14T SRAM is appeared in Fig_2. The transistors T14 and T1 is constrained by a word line (WL), are get to transistors, which

control the association between the bit line BL and BLB , accordingly the capacity hubs (Q and QB). The hubs M1 and M0 are repetitive hubs of Q and QB. On the off chance that the put away piece is "1," the rationale esteems at hubs Q="1", QB="0", M1="1,", M0="0," .

The practical investigation of the RHBD-14T SRAM is sequentially introduced: compose; read; and hold activity. In compose activity, we accept that Q = "1" and QB = "0" and along these lines the bit lines BL and BLB are set to "0" and "1," individually. When the WL is actuated, the value put away in Q and QB will be changed to "0" and "1," individually. at that point , once WL is released from "1" to "0 ", the new condition of the memory cell is put away.

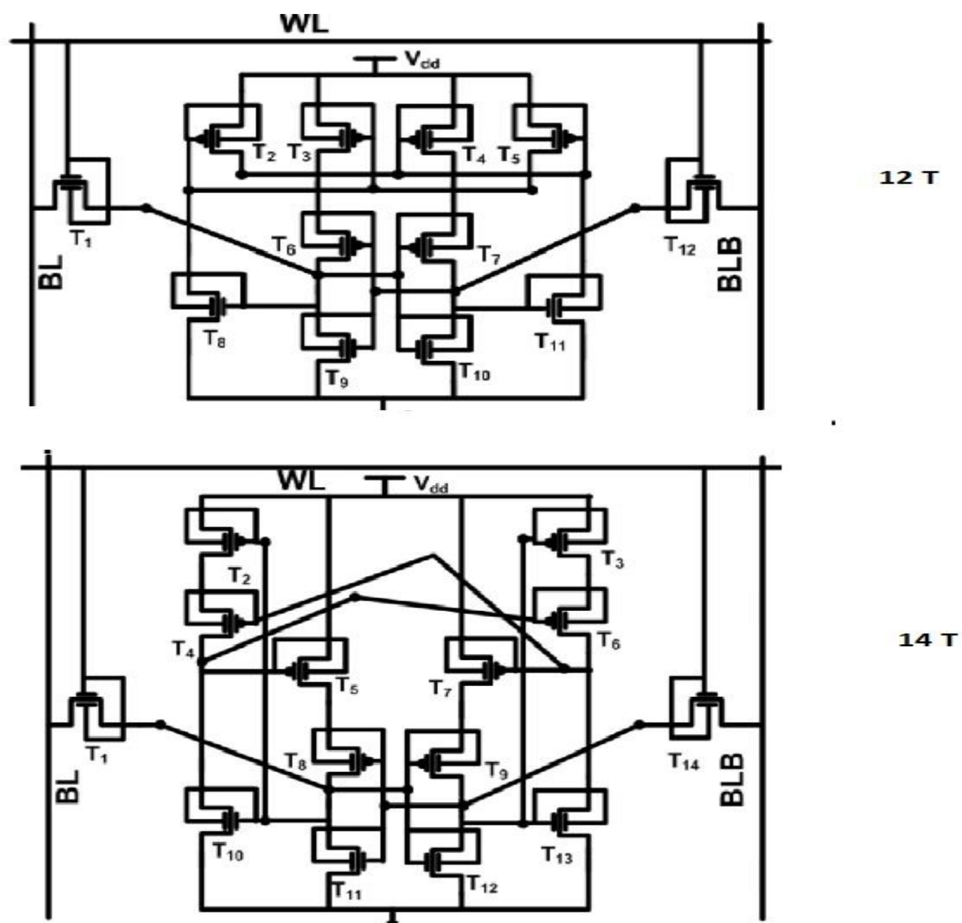

Figure 3.11: 12T and 14T SRAM bitcell

For a read activity, the BL and BLB are precharged to "1." When the picked WL is set off, the transistors T14 and T1 are turned on, BLB will be released to "0" through transistors T14 and T12. Therefore, the distinction voltage of the BLs will be created and intensified by the sense intensifier.

Throughout the hold action, WL is crippled then thusly the limit center points are disengaged from the BLs; therefore, they keep up the underlying state, the transistors T2 and T3 are wont to control the affiliation or cutoff between the workplace deftly and transistors T4/T6, which is useful to improve the speed of form and exhausted force differentiated and RHD-12T

CHAPTER 4

IMPLEMENTATION AND RESULTS

4.1 Implementation of Proposed Circuit:

A 14T SRAM cell from base paper [1] which is a radiation hardened structure is designed using MOSFET and FinFET in 22nm Technology. The software used is Synopsys HSPICE. Performance Metrics to be calculated:

Average Power Consumption, PDP, EDP and Delay

The proposed circuits using FinFET Technology for both 12T and 14T SRAM bitcell are shown in Figure 4.1 and 4.2.

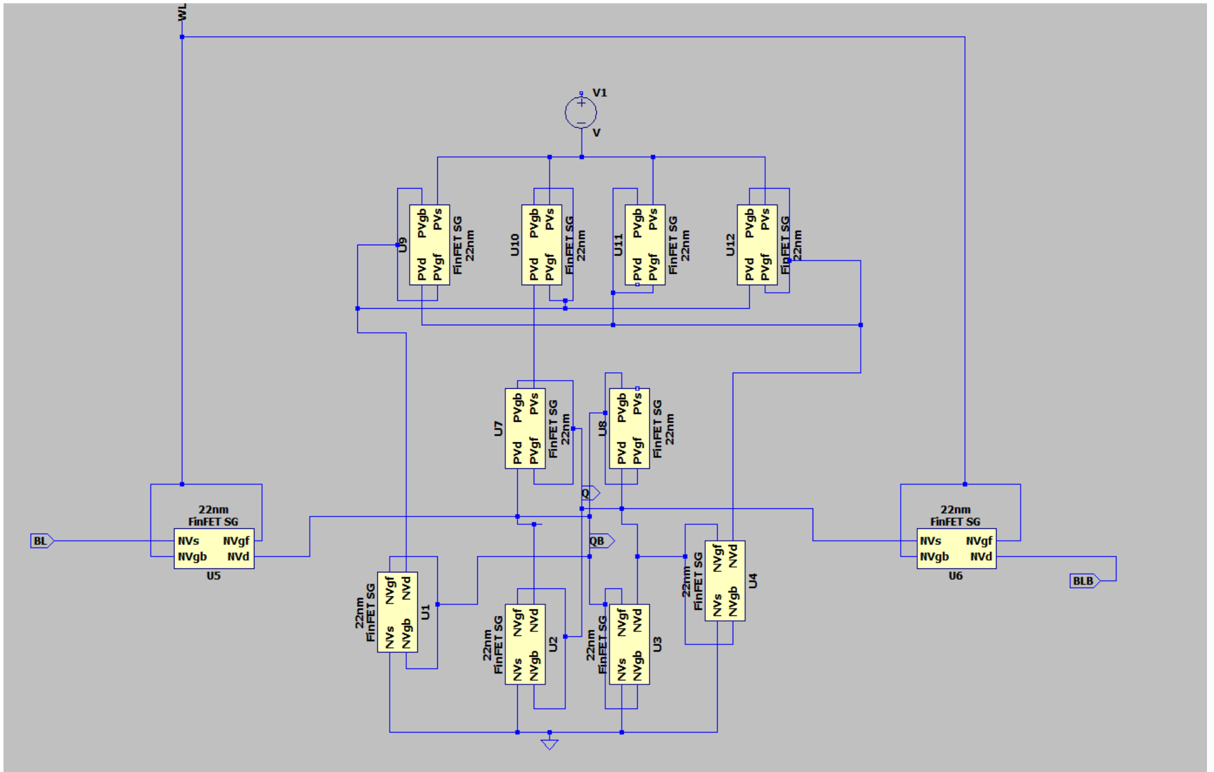

Figure 4.1: Proposed 12T SRAM Bitcell using FinFET 22nm

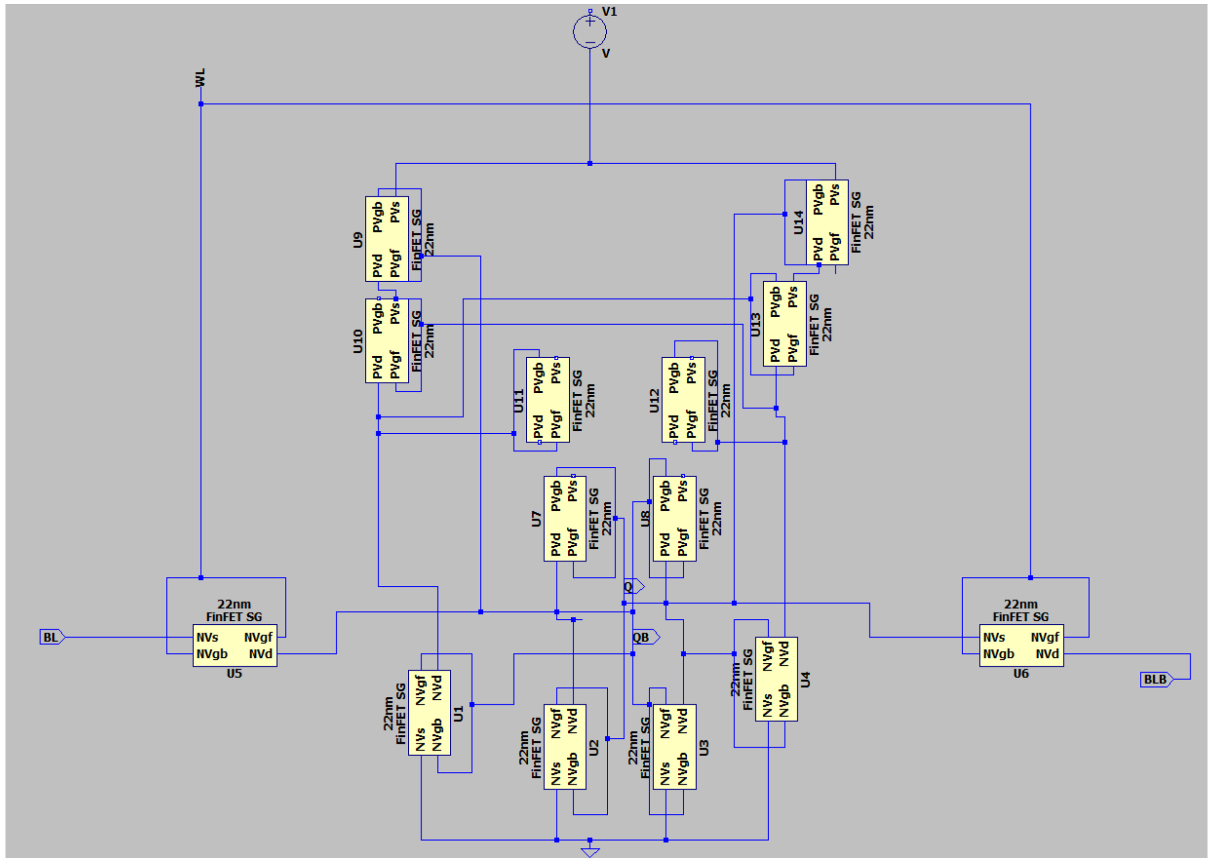

Figure 4.2: Proposed 14T SRAM Bitcell using FinFET 22nm

4.2 Proposed Methodology:

This chapter describes the methodology of the thesis; In this FinFET and SRAM based circuits are studied with utmost detail. The methodology consists of the following process:

- The tool used is Synopsys HSPICE.
- First circuit diagram is made on paper and then node numbers is added.
- Then MOSFET of FinFET configurations are written.
- The circuit netlist coding is added with proper analysis and results
- The circuit is then simulated with suitable FinFET model files.
- After simulation the input/output waveforms are checked for its validity
- Then parameter calculation commands are added
- The parameters calculated are Average Power Consumption, Delay, Power Dissipation and so on.
- All the circuits are implemented with this methodology
- All results are obtained and tabulated for graphical comparisons.
- This explains the methodology of the implementation in detail

- The technology used in this work is 22nm technology
- FinFET are used in shorted gate mode for high performance in terms of all performance metrics
- SRAM is tested under both MOSFET and FinFET based Circuits
- Existing Radiation Hardened 14T SRAM cells are studied and analysed in the results
- Proposed Circuit is analysed in all performance metrics and compared with existing circuits.
- The results are tested with transient response
- The results are evaluated on PULSE based inputs.
- The commands commonly used are tran for transient analysis

4.3 Results:

In this section, the results are mentioned. In figure 4.3, Average Power Comparison result for SRAM bitcell, it shows that when technology is shift from 32nm to 22nm. The average power consumption is increased, which is definitely because short channel effects.

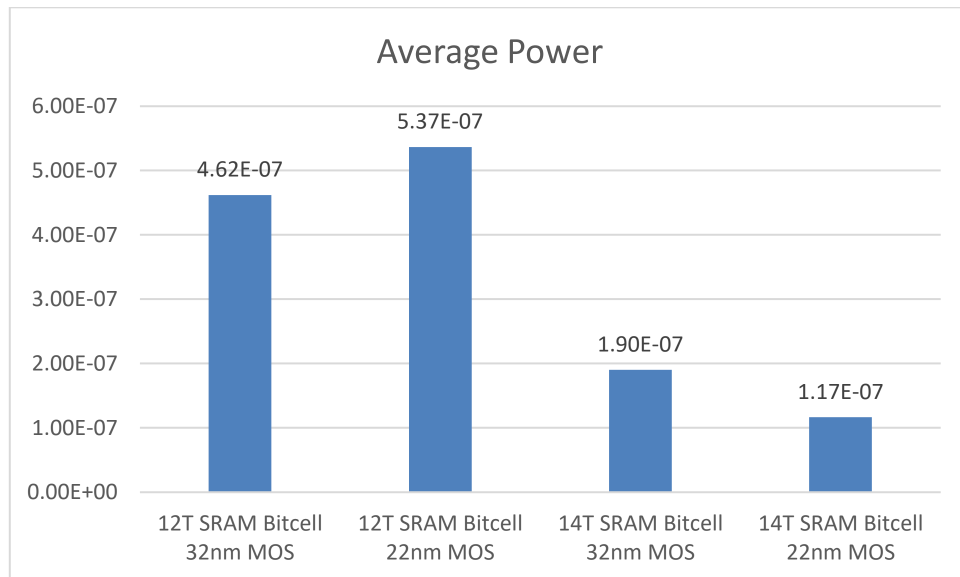

Figure 4.3: Average Power Comparison Result for SRAM Bitcell

Similarly, in figure 4.4, Delay comparison results indicate that 22nm technology circuits have high delay.

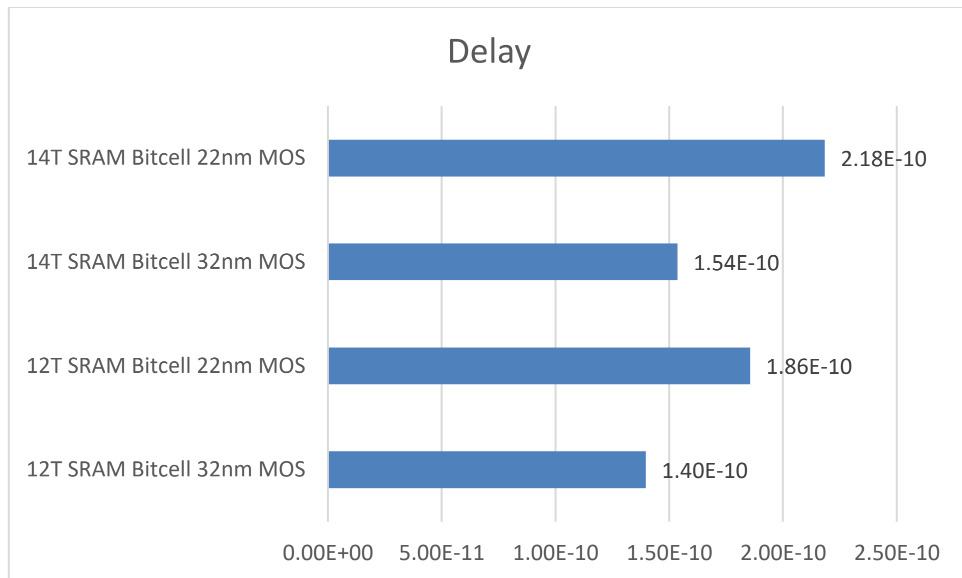

Figure 4.4: Delay Result for SRAM Bitcell

Now the proposed circuits given in figure 4.1 and 4.2, are implemented in FinFET 22nm technology. Figure 4.5 shows that Average Power is decreased by high percentage in the proposed circuits.

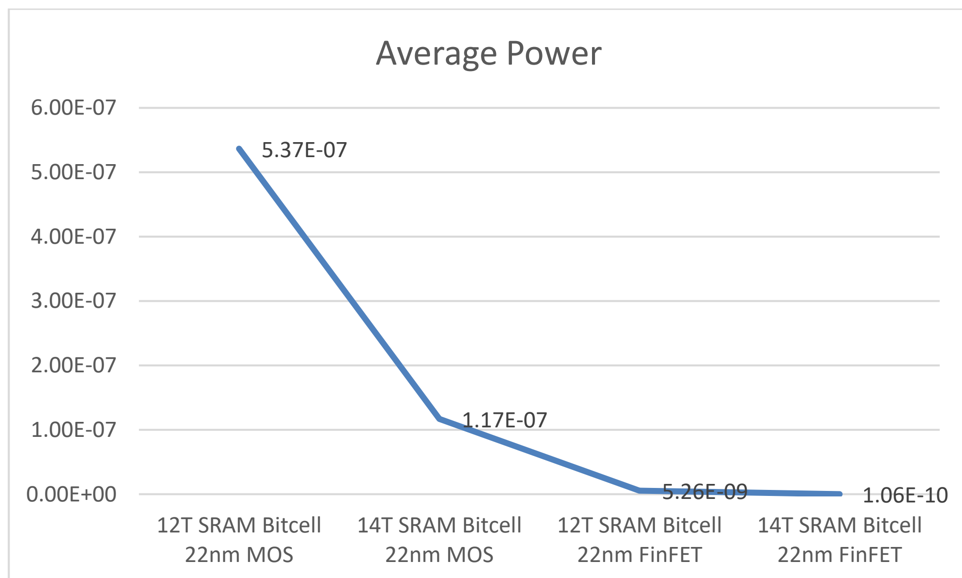

Figure 4.5: Average Power Comparison Result for SRAM Bitcell with Proposed FinFET

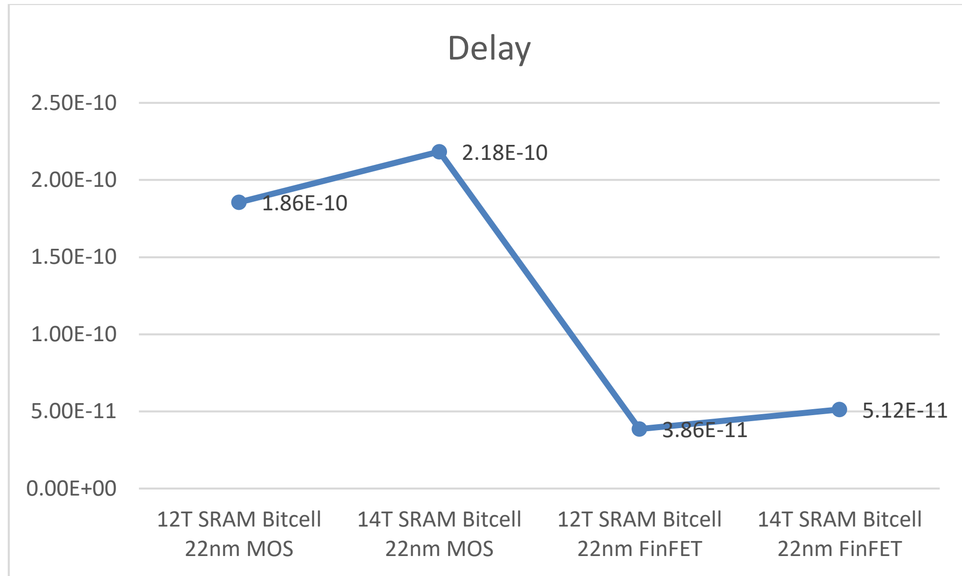

Figure 4.6: Delay Result for SRAM Bitcell with Proposed FinFET

Figure 4.6 shows that delay is reduced in proposed circuits. But delay is higher in case of 14T SRAM bitcell.

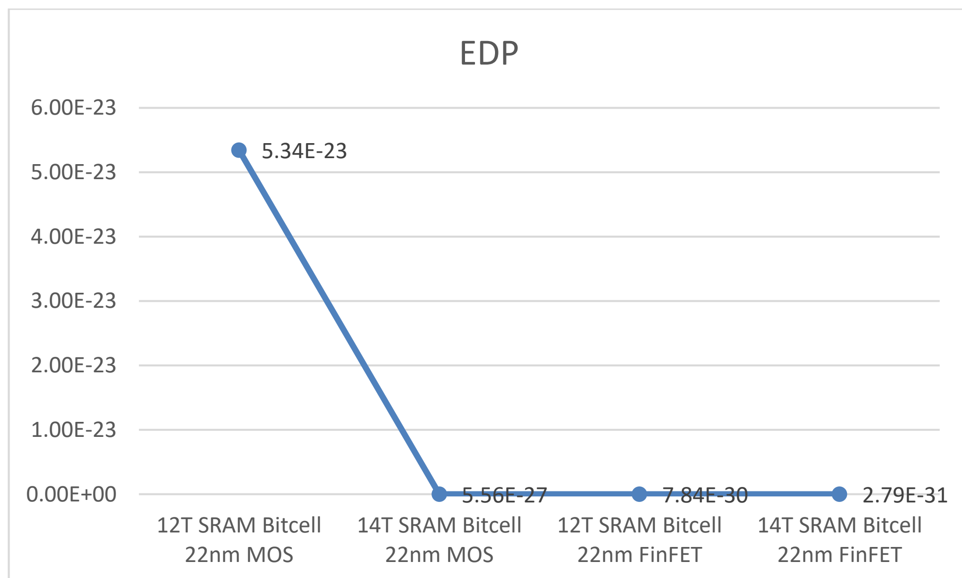

Figure 4.7: EDP Result for SRAM Bitcell with Proposed FinFET

Figure 4.7 and Figure 4.8 shows that the EDP energy delay product and PDP power delay product is also improved.

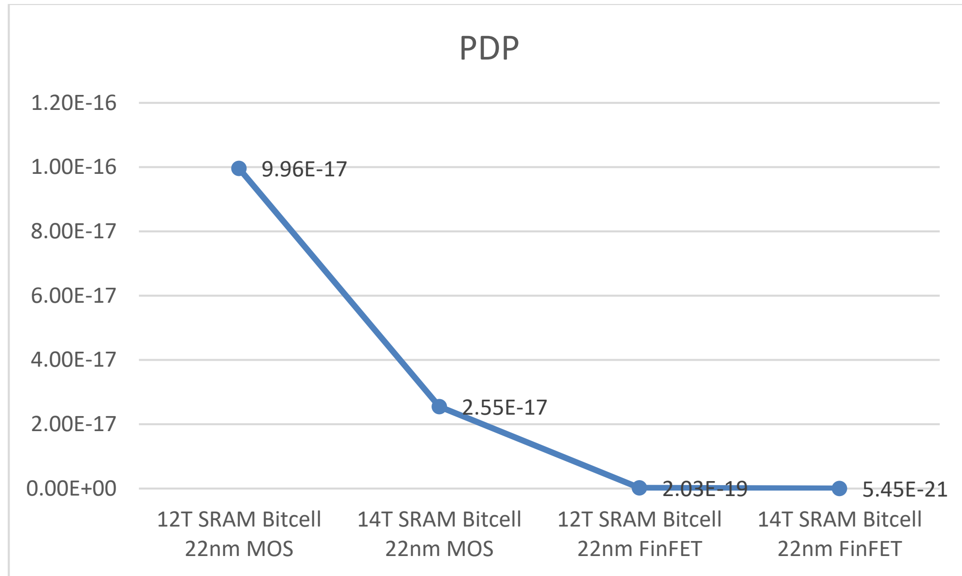

Figure 4.8: PDP Result for SRAM Bitcell with Proposed FinFET

In table 4.1 below, the simulation results parameters are mentioned in tabular format.

Table 4.1: Simulation Output Results

	12T SRAM Bitcell 32nm MOS	**12T SRAM Bitcell 22nm MOS**	**14T SRAM Bitcell 32nm MOS**	**14T SRAM Bitcell 22nm MOS**
Average Power	4.62E-07	5.37E-07	1.90E-07	1.17E-07
Delay	1.40E-10	1.86E-10	1.54E-10	2.18E-10
	12T SRAM Bitcell 22nm MOS	**14T SRAM Bitcell 22nm MOS**	**12T SRAM Bitcell 22nm FinFET**	**14T SRAM Bitcell 22nm FinFET**
Average Power	5.37E-07	1.17E-07	5.26E-09	1.06E-10
Delay	1.86E-10	2.18E-10	3.86E-11	5.12E-11
PDP	9.96E-17	2.55E-17	2.03E-19	5.45E-21
EDP	5.34E-23	5.56E-27	7.84E-30	2.79E-31

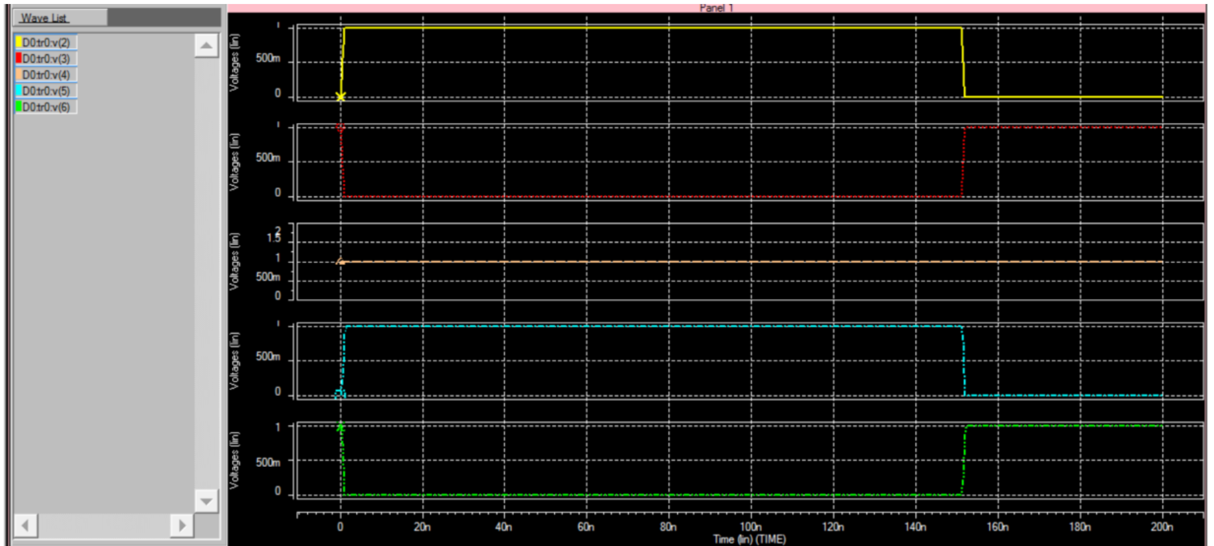

Figure 4.9: MOSFET SRAM Waveform

In figure 4.9, the waveform of signals BL, BLBar , WL, Q and Qbar are presented for MOSFET based SRAM and Similarly in figure 4.10 the waveforms are given for FinFET based proposed SRAM bitcell for 12t and 14t based SRAM bitcell.

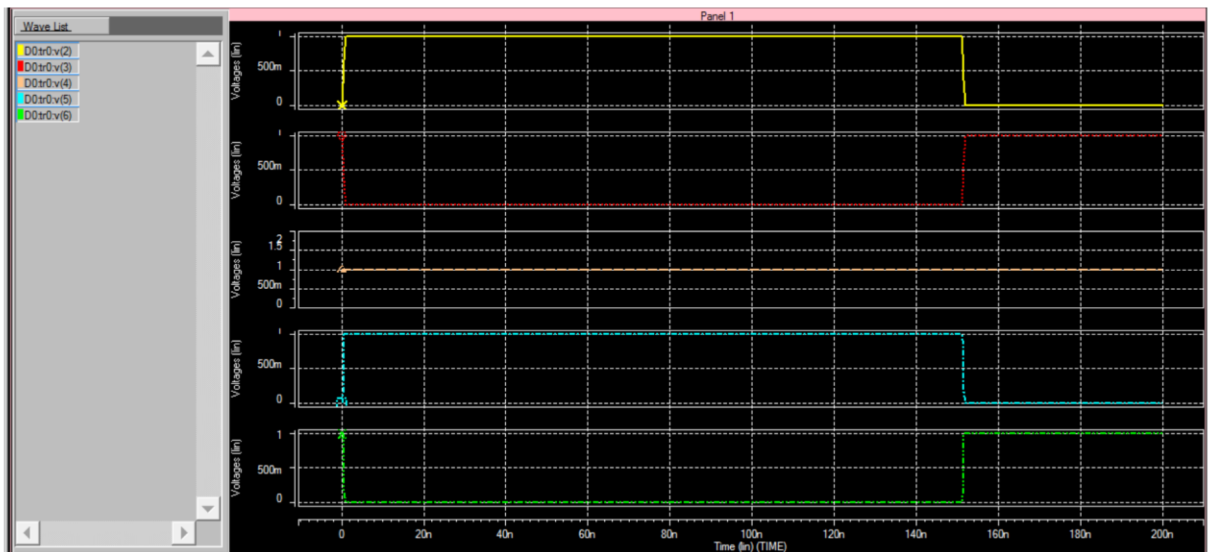

Figure 4.10: FinFET Proposed Waveform

CHAPTER 5
CONCLUSION

5.1 Conclusion:

Thus, reason that by utilization of FinFET transistor among Radiation Hardened Bitcell SRAM will improve the qualities and execution of the circuit. The proposed circuit comprises of 14T based FinFET. The improvement in the circuit are follows:

In proposed circuit 12t SRAM:

- Average power consumption is decreased by 99%,
- PDP is improved by 99.7%
- EDP is decreased by 99%
- propagation delay is improved by 79.2%,

In proposed circuit 14t SRAM based improvements are:

- 99% in Average Power consumption
- 76.5% in propagation Delay
- 99.4% in PDP
- 99.5% in EDP

5.2 Future Scope:

FinFET area unit extremely a necessary step within the evolution of semiconductors simply because bulk CMOS has difficulties in scaling on the far side 32 nm. Use of the back gate it becomes a very attention-grabbing design opportunities. made diversity of style designs, created potential by freelance management of FinFET gates, may be used efficiently to cut back consumption of total active power IG/LP mode circuits give an encouraging exchange between power and area. Further future scope of improvement can be the use of the independent gate design of FinFET. In future, this work can be further extended with the use of other transistor technologies.

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Appendix

FinFET Parameters and Model:

The BSIM-CMG Model:

The current demonstrating endeavors for the multi-gates FETs are restricted to undoped or delicately doped silicon body for twofold entryway (DualGate) FETs. A various limit power innovation dependent on normal entryway multi-door FETs will probably need a noteworthy grouping of body dopant for edge voltage tuning. Thus, BSIM-CMG models the outcome of limited body doping on the electrical attributes of a multi-entryway FET in Poisson's condition. Beginning from a center long-channel symmetric DG-FET system, the model is reached out to significantly increase entryway FinFETs and fourfold door FinFETs through 3-D displaying of SCE. An extraordinary field scattering length model is created to catch the more grounded electrostatic power over the channel because of numerous doors, which prompts decreased subthreshold spillage in multigate FETs. Normal door multi-entryway FETs can be made on SOI or mass silicon. BSIM-CMG permits the client to choose SOI mode or mass SOI type through the expansion of the structure hub for mass multi-door FET. The BSIM-CMG potential model has been effectively used to portray the deliberate electrical attributes of SOI types FinFETs and mass FinFETs.

BSIM-CMG is a surface potential based model. Each and every electrical variable, for instance, terminal streams, charges and capacitances are gotten from the surface limits at the channel and the source end. The tally of the surface prospects outlines the reason of the model. The focal point of the model for BSIMCMG is a Double-Gate long_channel FET model. Plenteous physical miracles found in an imaginative Multigate FET advancement are significantly added model to yield the last model. The fragment delineates the BSIM-CMG model development. The focal point of the model is previously advanced by separating the direct of a long-channel DGFET. Next, exhibiting of a part of the huge semiconductor impacts, for instance, QME, SCE and PDE are portrayed. The region finally closes with the check of the model against exploratory data.

List of physical effects modeled in BSIM-CMG:

1) Quantum Mechanical Effects

2) Short-channel Effects

a) Vth roll-off

b) DIBL

c) Sub-threshold slope

d) Channel length modulation

3) Polysilicon-gate Depletion Effects (PDE)

4) Series resistance

5) Mobility degradation

6) Velocity Saturation

7) Velocity Overshoot/Source-End Velocity Limit

8) Gate Induced Drain (Source) Leakage (GIDL, GISL)

9) Impact Ionization

10) S/D Junction leakage

11) Gate tunneling

12) Parasitic capacitance

All the physical impacts remembered for BSIM-CMG are recorded previously. The absolute most significant physical impacts are talked about straightaway. As instances of the physical impact models, the accompanying subsections present the quantum mechanical impact model and the short-divert impact model in certain subtleties.

Technology Used: 22nm

Model Files: 22nmfinfet.pm

```
* This  is sub 22nm FinFET predictive model
.options   post=2   brief
.paramtbsi=8.6n

**   subckt   for   NMOS   **

.subckt   DGNMOS   NVdNVgfNVgb   NVs   wdg=80n   ldg=22n
.include   './soinmos1.pm'     *   front   soi   model   card
.include   './soinmos2.pm'     *   back   soi   model   card
.parampnch   =   2e16
```

```
.paramptox = 1.4e-9
.paramptsi = 'tbsi'
.paramptbox = 1.4e-9
.param npvthf0 = 0.29
.param npvthb0 = 0.29
.paramesi = 11.7
.parameox = 3.9
.param nlambda1 ='(-1)*( ptox / (ptbox + ptsi /(esi/eox)))'
.param nlambda2 ='(-1)*( ptbox / (ptox + ptsi / (esi/eox)))'
.param delta1 = 0.008
.param delta2 = 0.008
.param Voff2=-0.09
.param N = 0.2
.paramVt = 0.0259
.param Voff1 = 0.0
mn1 NVd NVgf1 NVs 0 nmos1 w='wdg/2' l='ldg'
+ as='wdg / 2 * 2 * ldg' ad='wdg / 2 * 2*ldg'
+ ps='wdg/2+4*ldg' pd='wdg/2+4*ldg'
mn2 NVd NVgb1 NVs 0 nmos2 w='wdg/2' l='ldg'
+ as='wdg/2*2*ldg' ad='wdg/2*2*ldg'
+ ps='wdg/2+4*ldg' pd='wdg/2+4*ldg'
En1 NVgf NVgf1 VOL = 'nlambda1*(-1*N*Vt*log(1+exp((((nlambda2*(npvthb0-
(v(NVd)-v(NVs))*delta2)+(npvthf0-(v(NVd)-v(NVs))*delta1))/(1-
(nlambda1*nlambda2))+Voff2)-(v(NVgb)-v(NVs))-
Voff1)/N/Vt))+N*Vt*log(1+exp((((nlambda2*(npvthb0-(v(NVd)-
v(NVs))*delta2)+(npvthf0-(v(NVd)-v(NVs))*delta1))/(1-(nlambda1*nlambda2))+Voff2)-
Voff1)/N/Vt))-1*N*Vt*log(1+exp(((-1)*((nlambda2*(npvthb0-(v(NVd)-
v(NVs))*delta2)+(npvthf0-(v(NVd)-v(NVs))*delta1))/(1-(nlambda1*nlambda2))+Voff2)-
Voff1)/N/Vt))+N*Vt*log(1+exp((-Voff1)/N/Vt)))'
En2 NVgb NVgb1 VOL = 'nlambda2*(-1*N*Vt*log(1+exp((((nlambda1*(npvthf0-
(v(NVd)-v(NVs))*delta1)+(npvthb0-(v(NVd)-v(NVs))*delta2))/(1-
(nlambda1*nlambda2))+Voff2)-(v(NVgf)-v(NVs))-
Voff1)/N/Vt))+N*Vt*log(1+exp((((nlambda1*(npvthf0-(v(NVd)-
v(NVs))*delta1)+(npvthb0-(v(NVd)-v(NVs))*delta2))/(1-(nlambda1*nlambda2))+Voff2)-
```

```
Voff1)/N/Vt))-1*N*Vt*log(1+exp(((-1)*((nlambda1*(npvthf0-(v(NVd)-
v(NVs))*delta1)+(npvthb0-(v(NVd)-v(NVs))*delta2))/(1-(nlambda1*nlambda2))+Voff2)-
Voff1)/N/Vt))+N*Vt*log(1+exp((-Voff1)/N/Vt)))'
.ends

** sub ckt for PMOS **

.subckt DGPMOS PVdPVgfPVgbPVs  wdg=1u ldg=22n
.include './soipmos1.pm' * front soi model card
.include './soipmos2.pm' * back soi model card
.parampnch =2e16
.paramptox = 1.4e-9
.paramptsi = 'tbsi'
.paramptbox = 1.4e-9
.param ppvthf0 = -0.25
.param ppvthb0 = -0.25
.paramesi = 11.7
.parameox = 3.9
.param plambda1 ='(-1)*(ptox/(ptbox+ptsi/(esi/eox)))'
.param plambda2 ='(-1)*(ptbox/(ptox+ptsi/(esi/eox)))'
.param pdelta1 = 0.008
.param pdelta2 = 0.008
.param Voff2 = 0.12
.param N = 0.2
.paramVt = 0.0259
.param  Voff1  =  0.0
mp1  PVd  PVgf1 PVs  n1  pmos1 w='wdg/2' l='ldg'
+ as='wdg/2*2*ldg' ad='wdg/2*2*ldg'
+ ps='wdg/2+4*ldg' pd='wdg/2+4*ldg'
mp2  PVd  PVgb1 PVs  n1  pmos2 w='wdg/2' l='ldg'
+ as='wdg/2*2*ldg' ad='wdg/2*2*ldg'
+ ps='wdg/2+4*ldg' pd='wdg/2+4*ldg'
vvdd n1 0 1
```

```
Ep1 PVgf PVgf1 VOL = 'plambda1*(-1*(-1*N*Vt*log(1+exp((-1*((plambda2*(ppvthb0-
(v(PVd)-v(PVs))*pdelta2)+(ppvthf0-(v(PVd)-v(PVs))*pdelta1))/(1-
(plambda1*plambda2))+Voff2)+(v(PVgb)-v(PVs))+Voff1)/N/Vt))+N*Vt*log(1+exp((-
1*((plambda2*(ppvthb0-(v(PVd)-v(PVs))*pdelta2)+(ppvthf0-(v(PVd)-
v(PVs))*pdelta1))/(1-(plambda1*plambda2))+Voff2)+Voff1)/N/Vt))-
1*N*Vt*log(1+exp((((plambda2*(ppvthb0-(v(PVd)-v(PVs))*pdelta2)+(ppvthf0-(v(PVd)-
v(PVs))*pdelta1))/(1-
(plambda1*plambda2))+Voff2)+Voff1)/N/Vt))+N*Vt*log(1+exp((Voff1)/N/Vt))))'
Ep2 PVgb PVgb1 VOL = 'plambda2*(-1*(-1*N*Vt*log(1+exp((-1*((plambda1*(ppvthf0-
(v(PVd)-v(PVs))*pdelta1)+(ppvthb0-(v(PVd)-v(PVs))*pdelta2))/(1-
(plambda1*plambda2))+Voff2)+(v(PVgf)-v(PVs))+Voff1)/N/Vt))+N*Vt*log(1+exp((-
1*((plambda1*(ppvthf0-(v(PVd)-v(PVs))*pdelta1)+(ppvthb0-(v(PVd)-
v(PVs))*pdelta2))/(1-(plambda1*plambda2))+Voff2)+Voff1)/N/Vt))-
1*N*Vt*log(1+exp((((plambda1*(ppvthf0-(v(PVd)-v(PVs))*pdelta1)+(ppvthb0-(v(PVd)-
v(PVs))*pdelta2))/(1-
(plambda1*plambda2))+Voff2)+Voff1)/N/Vt))+N*Vt*log(1+exp((Voff1)/N/Vt))))'
.ends
X1 nd vg1 vg1 0 DGNMOS
*X2 nd vg1 vg1nvdd DGPMOS
vvddnvdd 0 0.9
vfg vg1 0 0
vdnd 0 0.05
.op
.dc vfg 0 0.9 0.1
.print i(vd)
.end
```

List of Publications

[1] **Rajesh Kumar Raushan**, Mohammad Rashid Ansari ,Usha Chauhan, Muhammad Khalid,"Implementation of 12T and 14T SRAM bitcell using FinFET with optimized parameters", Transactions on Electrical and Electronic Materials (TEEM), Springer Nature (Submitted)

[2] **Rajesh Kumar Raushan**, Mohammad Rashid Ansari and Usha Chauhan and, "An Assessment on SRAM using MOSFET and FinFET Technology in VLSI", International conference on Smart, Machine Intelligence and Real-Time Computing ,2020 SMARTCOM 2020, (Accepted)