A

Thesis

On

OPTIMIZATION OF DYNAMIC CLOCK BASED D FLIP FLOP FOR LOW POWER APPLICATION

Submitted in partial fulfilment of the

requirement for the award of the

Degree of

MASTER OF TECHONOLOGY

in

VLSI Design

by

Shruti Shrivastava (1515108001)

Under the Supervision of

Dr. Usha Chauhan
(Associate Professor, Electronics and Communication Engineering)

SCHOOL OF ELECTRICAL, ELECTRONICS AND COMMUNICATION ENGINEERING

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DECLARATION

I declare that the work presented in this report titled "**OPTIMIZATION OF DYNAMIC CLOCK BASED D FLIP FLOP FOR LOW POWER APPLICATION**", submitted to the Department of Electronics and Communication Engineering, SEECE, Galgotias University, Greater Noida, for the Master of Technology in VLSI Design is our original work. We have not plagiarized unless cited or the same report has not submitted anywhere for the award of any other degree. We understand that any violation of the above will be cause for disciplinary action by the university against us as per the University rule.

Place:

Date:

Signature of the Student

_____

Shruti Shrivastava (1515108001)

School of Electrical, Electronics and Communication Engineering

CERTIFICATE

This is to certify that the project titled **"Optimization of Dynamic Clock based D Flip Flop for Low Power Application''** is the bonafide work carried out by Shruti Shrivastava, during the academic year 2019-20. We approve this project for submission in partial fulfilment of the requirements for the award of the degree of Master of Technology in VLSI Design, SEECE, Galgotias University.

Dr. Usha Chauhan

Project Guide(s)

The Project is Satisfactory / Unsatisfactory.

_____ _____

Internal Examiner (s) External Examiner

Approved by

_____

Dean

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ABSTRACT

D flip flop are of basic two types- static and dynamic. This thesis focuses on dynamic D flip flop. The dynamic nature comes with clock and reset configuration in TSPC (True single phase clocked). The clock and rest signal consume a lot of power when it comes to its work and switching activity. This makes it an important research area where it is necessary to improve the power consumption of the TSPC based D flip flop. Below 22nm, due to effects like DIBL or GIBL, power consumption rises, which also needs to improve. In this thesis, a new TSPC based D Flip Flop is proposed for low power application with MTCMOS (Multi-Threshold CMOS Logic) sleep signal insertion to reduce the power consumption for low power applications. This works uses low power based MOS like GNRFET to reduce the short channel effects in MOS. This focusses on Low power by the use of GNRFETs in 22nm technology.

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GLOSSARY

D Delayed

VLSIVery Large-Scale Integration

DFF Delay Flip Flop

GNRFET Graphene Nano Ribbon Field Effect Transistor

MOSFET Metal Oxide Semiconductor Field Effect Transistor

Clk Clock

TSPC True Single-Phase Clock

MOS Metal Oxide Semiconductor

PDP Power Delay Product

MTCMOS Multi-threshold Complementary Metal Oxide Semiconductor

PET Positron Emission Tomography

ADC Analog-to-Digital Converter

PMOS Positive channel Metal Oxide Semiconductor

UMC United Microelectronics Corporation

CMOS Complementary Metal Oxide Semiconductor

MSB Most Significant Bit

SPICE Simulation Program with Integrated Circuit Emphasis

BGB Bistable Gated Bipolar Device

DTMOS Dual-threshold Complementary Metal Oxide Semiconductor

PVTProcess-Voltage-Temperature

EDP Energy-Delay-Product

NMOSNegative channel Metal Oxide Semiconductor

ULSI Ultra Large-Scale Integration

GNRGraphene Nano Ribbon

SBFETSchottky obstacle field-influence transistor

NEGFNon-Equilibrium Greens Function

CNT Carbon Nanotubes

Si Silicon

FinFET Fin Field Effect Transistor

CNFET Carbon Nanotubes Field Effect Transistor

SRAM Static Random-Access Memory

IC Integrated Circuit

RCA Ripple Carry Adder

PG Power Gating

CAD Computer Aided Design

VCOVoltage-Controlled Oscillator

Chapter 1
INTRODUCTION

1.1 INTRODUCTION

D flip-flop is considered to be the most fundamental memory cell in by far most of digital circuits, which brings it broad use, particularly under current conditions where high-density pipeline innovation is every now and again employed in digital integrated circuits and gigantic flip-flop modules are indispensable segments. As a constant research centre, various different sorts of zero flip-flops have been invented and investigated, and the ongoing exploration trend has turned to rapid low-control execution, which can be boiled down to low power-delay product. To actualize superior VLSI, picking the most suitable D flip-flop has clearly become a very noteworthy part in the design stream. The reasons originate from two viewpoints: one is that 0 flip-flop has direct impact on the clock recurrence of digital circuit frameworks, particularly for some small scale structures with shallow sensible depth, the other one is that 0 flip-flop is an indispensable segment of clock organize, which tends to expend 30%-half of the force dissipation of the entire chip. According to the past looks into, some regular D flip-flops with magnificent execution have been presented. As a regular occurrence, the Pulse sans generator Hybrid Latch based Flip-Flop (DFF) proposed in has considerably reduced the basic way delay and shrewdly removed the beat generator unit, which brings about a usage of semi static circuit and a distinct advantage as far as both speed and force dissipation. In our work, DFF has been reinvestigated and modified as a fundamental structure. From another perspective, with the innovation downsizing, spillage power dissipation has become an increasingly more significant piece of all out force dissipation, and a few run of the mill new devices have been proposed to take care of this issue. Up until now, GNRFET is by all accounts the most encouraging new device, and business chips have already been released by significant foundries. Right now, is employed to substitute planar MOSFET to improve the presentation of DFF. In the interim, considering the advantages of numerous working modes of GNRFET, DFF is modified to accomplish lower power dissipation without an excessive amount of misfortune on working speed.

The working of D flip flop is like the D lock with the exception of that the yield of D Flip Flop takes the condition of the D contribution right now of a positive edge at the clock pin (or negative edge if the clock input is dynamic low) and delays it by one clock cycle. That is the reason, it is regularly known as a delay flip flop. The D Flip-flop can be interpreted as a delay line or zero order hold. The advantage of the D flip-flop over the D-type "lock" is that the sign on the D input pin is captured the minute the flip-flop is clocked, and consequent changes on the D information will be ignored until the following clock occasion. At the point when a circuit is edge triggered the yield can change just on the rising or falling edge of the clock. Yet, on account of level-clocked, the yield can change when the clock is high (or low). In edge activating yield can change just at one moment during the lock cycle; with level timing yield can change during a whole half pattern of the clock. The customary D – Flip flop is the extremely fundamental design of DFF. Locks are regularly called level-touchy in light of the fact that their yield follows their contributions as long as they are enabled. They are inert during this whole time when the empower signal is asserted. There are circumstances when it is increasingly helpful to have the yield change just at the rising or falling edge of the empower signal. This empower signal is typically the controlling clock signal. Therefore, we can have all progressions synchronized to the rising or falling edge of the clock. An edge triggered DFF accomplishes this by consolidating in arrangement a couple of hooks. The primary lock is called the ace hook. The ace hook is enabled when Clk = 0 and follows the essential information D. When Clk is a 1, the ace hook is disabled yet the second lock, called the slave hook, is enabled with the goal that the yield from the ace hook is transferred to the slave lock. The slave hook is enabled at the same time that Clk = 1, yet its substance changes just toward the start of the cycle, that is, just at the rising edge of the sign on the grounds that once Clk is 1, the ace lock is disabled and so the contribution to the slave hook will not change. The ordinary DFF constructed with NAND gates is given beneath. It has four NAND gates through and through and an inverter. There are three districts of flip-flop activity, of which just a single locale is worthy for a consecutive design to work accurately.

The locales are:

• Stable locale: Where the arrangement and hold times of a flip-flop are met and the Clock-to-Q delay isn't dependent on the D-to-Clock delay. This is the required district of activity.

• Metastable: As D-to-Clock delay decreases, at one point the Clock-to-Q delay begins to rise exponentially and ends in disappointment. The Clock-to-Q delay is in deterministic and this

may cause irregular disappointments and practices which are difficult to debug in genuine circuits.

• Failure locale: Where changes in data can't be transferred to the yield of the flip-flop.

1.2 PROBLEM STATEMENT

Improved TSPC D flip-flops with low force delay product based on GNRFET have been presented right now. Based on the better electrical properties and one of a kind advantages of numerous working modes of GNRFET, reduces the force delay product. In the interim, the last additionally chops down the quantity of transistors, which makes it increasingly appropriate for elite digital ICs as the MOSFET mass has high short divert impacts in 32nm and beneath. This establishes the issue articulation of the proposition.

1.3 MOTIVATION

GNRFET has been introduced to the design of superior dynamic TSPC D flip-flops. Based on the incredible electrical properties of GNRFET, the TSPC D flip-flop modified from unique by subbing MOS like GNRFET for planar MOSFET has a tremendous reduction on power-delay product (PDP). Considering the novel benefits of various working modes of GNRFET, further streamlining based on Modified TSPC based on MOSFET like GNRFET has been proposed to accomplish lower PDP and progressively productive zone usage rate. The recreation results indicate that the Modified TSPC D Flip Flop reduces the PDP and marginally builds the quantity of transistors.

1.4 OBJECTIVE

Our main objectives are:

- To DESIGN the TSPC and Modified TSPC based D FLIP-FLOP WITH LOW POWER and PROPAGATION DELAY BASED ON GNRFET optimization.
- To implementing accurate and efficient system using GNRFET in dynamic DFF.
- To design less power consuming circuit, it prevents short circuit power consumption by using a MTCMOS transistor in circuit.
- To Design low power device which is now an essential field of research due to increase in demand of portable devices by adding MTCMOS technique.

- To design high speed conventional D flip-flop using GNRFET in 22nm Technology.

1.5 THESIS ORGANIZATION

The remaining thesis proposition is arranged out as follows:

Chapter 1 contains Introduction about D flip flop and need, objectives of this thesis.

Chapter 2-literature review of previous year papers

Chapter 3- GNRFET in detail

Chapter 4- D flip flop explanations in VLSI

Chapter 5-Implementation and result of GNRFET MTCMOS technique work

Chapter 6 conclusion and future scope is mentioned for GNRFET based Dynamic D Flip Flop

Chapter 2
LITERATURE REVIEW

2.1 RELATED WORK

[1]Jahangir Shaikh et. Al. Positron spread tomography (PET) is a nuclear helpful imaging method that makes a three-dimensional image of commonsense organs in the body. PET requires significant standards, speedy and low force multichannel easy to computerized converter (ADC). A regular multichannel ADC for PET scanner building contains a couple of squares. Most by far of the squares can be structured by using brisk, low force D flip-flops. A preset-competent certifiable single stage timed (TSPC) D flip-flop demonstrates different glitches (uproar) at the yield as a result of unnecessary flipping at the middle center points. Preset-competent adjusted TSPC (MTSPC) D flip flop have been proposed as an elective response for help this issue. Nevertheless, the MTSPC D flip-flop requires one extra PMOS to suspend flipping of the middle centers. Right now, structured a 7-piece preset-competent dark code counter by using the proposed D flip-flop. This work includes UMC 180 nm CMOS advancement for preset-skilled 7-piece dark code counter where we accomplished 1 GHz most noteworthy errand repeat with most imperative piece (MSB) defer 0.96 ns, control use 244.2 μW (miniaturized scale watt) and force delay thing (PDP) 0.23 pJ (Pico joule) from 1.8 V power supply.

[2] Naresh Kumar et al, this paper displays a novel D flip-flop for low voltage action with improved speed using SPICE reproduction; it misuses a dynamic cutoff voltage using DTMOS for ultra-low voltage task and a negative differential block amassing using Bistable Gated Bipolar Device (BGB). DTMOS gives low force usage and BGB gives quick due to less capacitance. So we have taken focal points of both the DTMOS and BGB gadget to make the D-Flip Flop for low force movement with rapid and low spillage current. Spillage is additionally decreased by alternative of two rest transistors.

[3] Himanshu Kumar et.al, There is enormous assortment experienced right now perspective on compelling scaling and procedure defects. So this paper oversees different D flip-flop circuits the extent that generosity and multiplication delay.

This work contemplates different realized D flip-flop circuits and after that perceives the circuit which is speediest when contrasted with others mulled over. Further, delay capriciousness appeared by circuits has been penniless down to test the immunity against PVT assortments for instance procedure, voltage and temperature. Right now, have researched the yield levels of different D flip-flop circuits. Push-pull partition D flip-flop demonstrates to be progressively productive when contrasted with different circuits regarding defer irregularity. The circuits have been mimicked using 32-nm advancement center point on SPICE. The structures offering least delay and its change are accounted for, to help the draftsman in picking the best arrangement dependent upon express requirements.

[4] M. Arunlakshman et al, Flip-Flop is an electronic circuit that stores a genuine condition of at any rate one data information banner considering a clock beat. During rehashing clock between times get and keep up data briefly period adequate for different circuits inside a system to additionally process data. Force dispersal is a noteworthy parameter in the structure of VLSI circuits, and the check framework is accountable for a considerable bit of it (up to 50%).When the inventory voltage is diminished the speed of the method of reasoning circuits might be lessened in light of decrease incapable data voltage to the transistors. The ideal inventory voltage for CMOS reason the extent that Energy-Delay-Product (EDP) is close to the edge voltage of the NMOS transistor Vtn for the genuine procedure, tolerating that the utmost voltage of the PMOS transistor Vtp is around proportionate to −Vtn .The notable Moore's law communicates that the amount of transistors that are to be incorporated on a single kick the basin gets multiplied for at standard interims and which demonstrates that area of the arrangement is in like manner an essential concern. From now on right now the three significant stresses of VLSI world, the force expended, speed and zone usage are concentrated.

[5] Huei Chaeng Chin et al, Comparative benchmarking of a graphene nano-ribbon field impact transistor (GNRFET) and a nano scale metal-oxide-semiconductor field-impact transistor (nano-MOSFET) for applications in ultra enormous scope joining (ULSI) is accounted for. GNRFET is observed to be indisputably unrivaled in the circuit-level building. The imperative vehicle properties of GNR actuate it into an elective development to evade the requirements forced by the silicon-based gadgets. Developing GNRFET, using the

circuit-level demonstrating programming SPICE, displays advanced execution for computerized method of reasoning passages in 16 nm procedure advancement. The examination of these execution estimations joins imperativeness defer thing (EDP) and force delay thing (PDP) of inverter and NOR and NAND gates, confining the structure hinders for ULSI. The appraisal of EDP and PDP is completed for an interconnect length that scopes upto 100μm. An assessment, in perspective on the channel and gateway current-voltage (Id-VdandId-Vg), for sub-threshold swing (SS), channel induced hindrance cutting down (DIBL), and current on/off extent for circuit execution is given. GNRFET can overcome the short-channel impacts that are inescapable in sub-100 nm Si MOSFET. GNRFET gives diminished EDP and PDP one solicitation of degree that is lower than that of a MOSFET. Despite the way that the GNRFET is imperativeness viable, the circuit execution of the gadget is restricted by interconnect capacitances.

[6] N.D. Akhavan et al, right now look at the presentation of reliably doped graphene nano-ribbon FET (GNRFET). Three dimensional quantum mechanical reenactments dependent on the NEGF formalism have been utilized inside seeing electron-phonon collaboration to mull over the exhibition of GNRFET. We discovered that consistently doped GNRFET expands the compactness and execution of GNRFET gadget stand out from ordinarily un-doped graphene.

[7] Yijian Ouyang et.al Scaling Behaviors of Graphene Nano-ribbon FETs: A Three Dimensional Quantum Simulation Study. The scaling of graphene nano-ribbon (GNR) Schottky obstacle field-influence transistors (SBFETs) are pondered by comprehending and isolating the non-balance Green's capacity (NEGF) transport condition in an atomistic explanation set with a three-dimensional Poisson condition. The rocker edge GNR channel circuit awards similarities to a befuddle CNT; in any case it has another fundamental geometry and quantum restraint cut-off condition the transverse way. The outcomes displays that the I-V qualities are ambipolar and generally depend upon the GNR width as the band hole of the GNR is conflictingly in regard to its width, which according to nonstop starters. A different gateway right hand geometry improves and redesigns insurance from short channel impacts; in any case it offers less improvement when diverged from Si MOSFETs seeing the on-current also as transconductance. Diminishing the oxide thickness completely is more critical for improving transistor execution than utilizing a high-κ door defender. Essential increase of the inconsequential spillage current is seen when the channel length is scaled underneath 10 nm as the little appropriate mass empowers solid source-channel burrowing.

The GNRFET, therefore, does not so much add to extending a definitive scaling cut-off of Si MOSFETs. The trading pace of a GNR SBFET is two or multiple times quicker than that of Si MOSFETs, which could add to promising brisk gear applications, where the enormous spillage of GNR SBFETs is of less concern.

[8] Abhijith A Bharadwaj et.al Design and Performance Comparison of FinFET, CNFET and GNRFET based 6T SRAM Static Random Access Memory (SRAM) has from long the most ideal approach to deal with store data electronically on-chip, in speedy circuits. The focal points of low zone, quick ICs are the duty of MOSFET scaling systems. Reasons for limitation on MOSFET scaling, results a need for new transistor development. Here it gives three SRAM (6T) cell models (Graphene Nano-ribbon FET, Multi-walled CNT FET and MOSFET) which give the course for advancement. The parameters as Read delay, Write deferral and Power-defer thing are contemplated. All the three developments, 10nm passage length is taken. Plan and expansion of a full scale SRAM cell is then considered (6T SRAM cell, Sense intensifier, Precharge circuit, Read and Write circuits) to give control assessment between 32X8, 32X16, 64x8 and 64x16 SRAM gatherings. Circuit is organized and re-establishment was done utilizing HSpice and CosmosScope.

[9] Praveena Kumari et.al Design and Analysis of 16bit Ripple Carry Adder and Carry Skip Adder Using Graphene Nano Ribbon Field Effect Transistor (GNRFET) Moore's law can't be considered extra. Since MOSFET's can't be scaled beneath 10nm due to its physical and partner properties .This trade-off outcomes in a route for new material used in fetes to be according to Moore's law. Distinctive different innovations include Carbon Nano-Tube FET (CNTFET), Fin-Shaped FET (FinFET), Reconfigurable Logic ,Reversible Logic, and Grapheme Nano-Ribbon FET (GNRFET), among the accessible headways GNRFET's Has demonstrated to be an inside and out promising potential substitution as far as design region, quicker activity, lower power utilization. Carbon is can be used in wide scale applications on the grounds that regardless of whether some material is made up of carbon molecules, it can have different attributes and morphologies depending on how carbon particles bind together. Sorting out of RCA and Cska adders utilizing GNRFET.

[10] Preetika Sharma et.al Effect of temperature on conductivity of GNRFET Graphene nano ribbons are the layers and areas of graphene sheet which has open band hole in graphene. This opening of band hole redesigns the on off degree of GNR contraptions and add to its utilization in method of thinking circuit applications. GNR in transistors give long range

applications in these zones. A GNRFET shows monstrous conductance with door voltages. The impact of temperature on this conductance in GNRFET is found right now impersonating and organizing a GNRFET model in VNL. A GNRFET with befuddle anodes and rocker channel is completely inspected. The conductance as for temperature is watched and recorded. A temperature degree of 0 to 2000 K is taken for the assessment.

[11] Huei Chaeng Chin et.al Enhanced Device and Circuit-Level Performance Benchmarking of Graphene Nano-ribbon Field-Effect Transistor against a Nano-MOSFET with Interconnects Graphene nano-ribbon field-influence transistor (GNRFET) and a nano scale metal-oxide semiconductor field-influence transistor (nano-MOSFET) for applications in ultra titanic scale joining (ULSI) is appeared. GNRFET supposedly is indisputably unmatched in the circuit-level execution and plan. The outstanding vehicle properties of GNR direct it into an elective development to ends imposed by the silicon-based devices. Developing GNRFET, utilizing the circuit level indicating programming SPICE, demonstrates upgraded execution for front line avocation gateways in16nmprocesstechnology.The evaluation of these introduction estimations joins centrality delay product(EDP) and force delay product(PDP) of inverter and NOR and NAND gates, framing the building obstructs for ULSI. The assessment of EDP and PDP is carried out for an interconnect length that reaches up to 100μm. An assessment, considering the channel and door current-voltage (Id-Vd and Id-Vg), for sub edge swing(SS),drain-started check chopping down (DIBL), and current on/off degree for circuit use is given. GNRFET can vanquish the short-channel impacts that are essential in sub-100nm Si MOSFET. GNRFET gives lessened EDP and PDP one requesting of essentialness that is lower than that of a MOSFET. Notwithstanding how the GNRFET is vitality skilled, the circuit execution of the device is obliged by the interconnect capacitances.

[12] Amit Sangal et.al GNRFET as future low force contraptions — the graphene nano-ribbon field influence transistor (GNRFET) is a making advancement that gotten a lot of thought beginning late. Late work on GNRFET circuit re-institutions has indicated that GNRFETs may have potential in low force applications. Right now, see the present work on GNRFET circuit appearing, consider the two game plans of GNRFETs, Metal-Oxide-Semiconducting-(MOS-)type and Schottky Barrier-(SB-)type GNRFETs, and absolute discussion about and investigate their particular qualities to the degree deferral, force, and

complain edge. Starting here of view, we talk about their potential applications, particularly the utilization towards low-control figuring. Our re-authorizations show that ideal (nonideal)MOS-GNRFETconsumes18%(35%)and54%(102%) all out force when diverged from top of the line (HP) Si-CMOS and low-control (LP) SiCMOS, only. SB-GNRFET does not adjust earnestly with MOSGNRFET to the degree control use. Regardless, faultless (non-immaculate) SB-GNRFET has 3% (5.4X) and 0.45% (83.5%) vitality concede thing (EDP) diverged from Si-CMOS (HP) and Si-CMOS (LP), independently, while ideal (non-ideal)MOS-GNRFET has 8% (93%) and 1.25% (14.3%) EDP appeared differently according to Si-CMOS (HP) and Si-CMOS (LP), only."

[13] Wan Sik Hwang Graphene Nano ribbon Field-Effect Transistors on Wafer-Scale Epitaxial Graphene on SiC substrates .We report the assertion of top-gated graphene nano-ribbon field influence transistors (GNRFETs) of ~10 nm width on tremendous zone epitaxial graphene demonstrating the opening of a band hole of ~0.14 eV. In spite of earlier impression of jumbled vehicle and absurd edge-ruthlessness impacts of GNRs, the exploratory outcomes presented here undeniably show that the vehicle instrument in deliberately made GNRFETs is standard band-transport at room temperature, and between band burrowing at low temperature. The whole space of temperature, size, and geometry ward transport properties and electrostatics of the GNRFETs are explained by a standard thermionic transmission and burrowing current model. Our joined test and indicating work shows that painstakingly made tight GNRs go about as regular semiconductors, and stay potential contender for electronic trading devices.

[14] Hader E. El-hmaily et.al High Performance GNR MTCMOS for low voltage CMOS Circuits a solid criticalness gating plan the use of Graphene Nano Ribbon discipline-influence Transistors (GNRFET) is proposed the use of 16nm development. The force Gating (PG) shape is made out of GNRFET as a centrality switch and MOS power gated module. The proposed shape settle the standard bothers of the standard PG position from the perspective extending the inducing delay and wake-up time in low–voltage domains. GNRFET/MOSFET Conjunction (GMC) is contracted to build different structures of PG; GMCPG-SS and GMCPG-NS. Along these lines to manhandling it to make multi-mode PG structures. Circuit assessment for CMOS quality gated fundamental leadership limit modules (ISCAS85 benchmark) of 16nm development is used to survey the demonstration of the proposed GNR centrality move is appeared differently corresponding to the traditional MOS one. Spillage quality, wake-up time and vitality concede thing are used generally speaking execution

circuit parameters for the evaluation. GMCPG-SS generally speaking execution results screen a reduction in spillage quality, concede time, and wake-up time, on standard as much as 88%, forty four%, and 24%, independently, and GMCPGNS structure diminishes the spillage quality amidst 69% and ninety two%, and wake-up time through 27-forty six% for extraordinary ISCAS85 hugeness gated modules then again with the MOSPG shape. Each multimode PG frameworks can diminish the spillage power stood out from the decision PG structures with movement inside the wake-up time by utilizing ninety nine percent."

[15] M. Akbari Eshkalak et.al Graphene Nano-Ribbon Field Effect Transistor under Different Ambient Temperatures This paper is the basic assessment on the impact of including temperature on the electrical attributes and high recurrent introductions of twofold gateway rocker graphene nano-ribbon field influence transistor (GNRFET). The outcomes diagram that the GNRFET under high temperature (HT-GNRFET) has the most raised cut-off rehash, least sub-edge swing, least trademark deferral and force delay thing differentiated and low-temperature GNRFET (LT-GNRFET) and medium-temperature GNRFET (MTGNRFET). In addition, the LT-GNRFET demonstrates the most immaterial off-state current and the most basic degrees of Ion/Ioff, run of the mill speed and adaptable charge. Additionally, the LT-GNRFET has the most basic door and quantum capacitances among three as of late referenced GNRFETs.

[16] Youngki Yoon et.al Performance Comparison of Graphene Nano-ribbon FETs with Schottky Contacts and Doped Reservoirs We present an atomistic 3D re-establishment take a gander at of the general execution of graphene nano-ribbon (GNR) Schottky hindrance (SB) FETs and transistors with doped stores (MOSFETs) by utilizing oneself steadfast answer of the Poisson and Schrödinger conditions inside the non-understanding green's trademark (NEGF) formalism. Immaculate MOSFETs show scarcely higher electrical execution, for each virtual and THz applications. The impact of non-idealities on mechanical gathering when everything is said in done execution has been examined, considering the closeness of single void, a territory brutality and ionized defilements close to the channel. All around, MOSFETs demonstrate additional solid properties than SBFETs. Territory disagreeableness and void issue, in a manner of speaking, impact when in doubt execution of both contraption types.

[17] Mayank Mishra et.al Performance improvement of GNRFET Inverter at 32nm development place point Moore's standard has been a vital benchmark for movements inside

the district of microelectronics and data dealing with. Believe it or not, it has played an instrumental situation in driving the field budgetary issues and dividing down of the trademark timespan has been the central system for improving the general execution of the contraption. regardless, as we keep up to abbreviate, closer to the nanometre ordinary, different segments like line edge mercilessness, burrowing results, unpredictable dopant variances, brief channel results, and so forward will all in all impact it's working and immediately, it's come to be of extraordinary substance to inspect other elective materials that may help expand the drenching Moore's law. a disaster area of studies is straightforwardly going inside the domain and a huge amount of chance advances like CNFETs, FINFETs, GNRFETs, and so forward are being examined. area impact transistors the utilization of Graphene Nano-Ribbons (GNRFETs) have created as promising period in light of their extraordinary provider shipping residences and limit concerning tremendous scope preparing and creation. This investigates the GNRFETs inverter all things considered execution with CMOS inverter at 32nm time place point. Ages show up about 2.5x upgrades inside the spread put off and 2x enhancements inside the force concede thing (PDP). Further movement of results changed into gotten by techniques for moving the degree of Nano-Ribbons along the edge of the stock voltage. On different the wide assortment of nano-ribbons it turned into saw that, impelling concede reduces, in the interim as extraordinary essentialness affirmation increments. In context on the derivation, the redesigned outcome changed into picked to be 15 nano-ribbons. The results recommend that that GNRFET is a promising decision for Si-CMOS, making it a top of the line recommendation to help expand the drenching Moore's standard.

[18] DEVENDRA UPADHYAY et.al Understanding the impact of graphene sheet fitting on the conductance of GNRFETs The impact of fitting the graphene sheets used as redirect in a graphene nano-ribbon field influence transistor (GNRFET) was researched. The view changed into executed utilizing self-standard answer of Poisson's and Schrodinger's condition in blend with non-balance green's trademark (NEGF) formalism. Graphene sheet channel become redone into extraordinary shapes and found that with the development of feature disagreeableness along the edge of GNR sheet the band opening of GNRFET channel increments. Fitting the channel reduces adaptability and transmission likelihood to a decision entirety and in like manner the introduction of I–V qualities of GNRFET ruins.

[19] Maedeh Akbari Eshkalak et.al Used Graphene nano-ribbon Field influence transistor with 2 door encasings. Right now door separators are offered in graphene field influence transistor which adds to the advantage of low and high dielectric constants."

[20] Nima Dehdashti Akhavan et.al Study of dependably doped graphene nano-ribbon transistor (GNR) FET utilizing quantum proliferation. Right now watch the general execution of dependably doped graphene nano-ribbon FET (GNRFET). 3-dimensional quantum mechanical augmentations based at the NEGF formalism had been used inside observing electron-phonon trade to analyze the general execution of GNRFET. We saw out that dependably doped GNRFET will manufacture the flexibility and execution of GNRFET device stand out from for the most part undoped graphene.

[21] Mihir R. Choudhury et.al Graphene Nano-ribbon FETs: Technology Exploration for Performance and Reliability Graphene nano-ribbon FETs (GNRFETs) are promising contraptions for past CMOS nano gadgets because of their mind blowing transporter transport properties and potential for huge scope dealing with and creation. This paper joins atomistic quantum-transport displaying with circuit re-sanctioning to perform advancement assessment for GNRFET circuits. Results demonstrate that GNRFETs offer essential additions over scaled CMOS at the 22-, 32-, and 45-nm focus focuses, with more than 26–144× improvement in the vitality delay thing at identical working center interests. A quantitative assessment of the impacts of collections and blemishes on the introduction and dependability of GNRFET circuits is besides presented. Re-establishment results show that anyway GNRFET circuits guarantee higher execution, lower centrality utilization, and in every way that really matters indistinguishable enduring quality at commensurate working fixations to scaled CMOS circuits, they are logically defenseless against collections and defects. These outcomes stir essential structure, outlining, and spread difficulties standing up to the contraption and PC upheld plan (CAD) social order connected with graphene gear investigate.

[22] Seyed Saleh Ghoreishi et.al Performance Evaluation and Design Considerations of Electrically Activated Drain Extension Tunneling GNRFET: A Quantum Simulation Study In this paper, a burrowing graphene nano ribbon field influence transistor with electrically instituted channel development, to be express, EA-T-GNRFET, is proposed. The proposed structure consolidates a side door at the channel side with a dependable voltage and length of

0.4 V and 15 nm, independently. Re-establishments are performed liable to the non-friendliness Green's capacity framework joined with the Poisson condition in the mode space depiction. This side passage makes an additional development in potential profile at the channel side, which enlargements and reduces the width of burrowing cutoff and spillage current, independently. In addition, the proposed structure has lower channel instigated block reducing, lower sub-edge swing (SS) and higher I ON/I OFF proportion than the standard structure. Also, different qualities of the device, for example, trading delay (ττ), control concede thing (PDP) and solidarity gain rehash (f t) are improved in the proposed contraption. These central focuses make EA-T-GNRFET constantly reasonable for forefront and straightforward applications."

[23] M. Arunlakshman et.al Effect of 15nm Graphene Nano Ribbon Field Effect Transistors (GNRFET) on Single Edge Triggered D – Flip Flop based Shift Registers and its association with 16nm MOSFET Technology. The observed Moore's law conveys that ―For reliably and a huge bit of the degree of transistors which may be to be melded on an kick the holder gets increased indefinitely‖. consequently the there exists a method implied as the scaling. MOSFET is one of the extraordinary transistors utilized in contemporary devices. The most discouraged piece of the MOSFET is that it can't be reduced underneath 10nm considering the manner in which that it impacts in the short channel results, wherein the channel an area between the source and the channel would be not prepared to lead charmingly. passed on to it, significance and speed additionally plays out a fundamental situation inside the VLSI development. For and structure the criticalness affirmation should be especially less and pace of should be to an additional volume. To beat this issues, another out of the plastic new transistor to substitution MOSFET for destiny gear should be researched to get higher outcomes in verbalizations of all the enormous show parameters like force, locale and pace.

[24] Wan Sik Hwang et al., Graphene nano ribbon field-influence transistors on wafer-scale epitaxial graphene on SiC substrates We report the attestation of top-gated graphene nano-ribbon field influence transistors(GNRFETs) of ~10 nm width on immense zone epitaxial graphene demonstrating the opening of a band hole of ~0.14 eV. Despite earlier impression of disarranged vehicle and silly edge-unpleasantness impacts of graphene nano-ribbons (GNRs), the primer results presented here clearly display that the vehicle instrument in carefully made GNRFETs is standard band-transport at room temperature and between band burrowing at low temperature. The whole space of temperature, size, and geometry ward transport properties and electrostatics of the GNRFETs are explained by an ordinary

thermionic radiation and burrowing current model. Our joined exploratory and displaying work shows that deliberately made thin GNRs carry on as standard semiconductors and stay potential contender for electronic trading contraptions.

[25] M.M Anas et al, A Study of Single Layer and Bilayer GNRFET Graphene Nano ribbons are among the beginning late discovered carbon nanostructures, with uncommon attributes for novel applications. A victor among the most important highlights of graphene Nano ribbons, from both head science and application perspectives, is their electrical band hole. Right now, consider the legitimacy of band opening in single and twofold layer Graphene nano ribbons (GNRs) of decided widths and edge geometries. The figuring's are finished utilizing Tight Binding quantum mechanical spreads for verifying the overhauled nuclear courses of action of the nano-ribbons and their electronic structures. Our estimations show that for single-layer graphene nano-ribbon with a width of 12A0, the one with rocker edge is semiconducting with a band hole of 0.25 eV while the one with screw up edge is metallic. For bilayer nano-ribbons, two specific stacking structures (AA and AB) are considered.

[26] Mr. Prathamesh G. Dhoble et al., An edge triggering device is a Delay (D) flip-flop.Using 32 nm CMOS technology, a high velocity, low energy usage, favorable edge triggered standard Delay (D) flip-flop can be intended to increase counter velocity in Phase closed loop.The standard D flip-flop has greater working frequencies but characteristics dissipation of static energy. The constructed counter can be used in the stage locked loop divider chip.In the feedback loop, a dividing counter is required to increase the frequency of VCO above the frequency of the input reference.The proposed circuit is going to be quicker than standard circuit as it is going to be a quick reset operation.The circuit will consume less energy because it avoids power consumption in the short circuit.

[27] Ms. Chaitali V. Matey et al., In contemporary VLSI devices such as Systems o Chips (SoCs), the development of high-performance and low-power clocked storage components is vital and critical to attaining maximum performance and reliability levels.TSPC D flip flop provides benefits over ordinary D flip flop design in terms of velocity and energy. Counters are sequential circuits that tract the amount of pulses that are applied to their inputs.They often happen in real-world, practical digital systems, with, to name a few, applications in computer systems, communication equipment, science tools, and industrial control.Many counter designs in literature, patents and/or practical use have been suggested.

[28] Prathamesh G et al., In today's global village, the use of low-power consumption appliances has become omnipresent and indispensable in almost every way of life. The aim is to decrease the high energy consumption needed to decrease circuitry costs while improving the performance speed in any operation. Write whatever you want A high speed low power consumption favourable edge caused Delayed (D) flip-flop can be designed with 32 nm CMOS technology to increase counter velocity in Phase closed loop. Here we design phase closed loop (PLL) D flip-flop.

[29] Jahangir Shaikh et al., Positron emission tomography (PET) is a method of nuclear functional imaging that generates a three-dimensional image of the body's functional organs. PET needs multichannel analog to digital converter (ADC) with high resolution, quick and low energy. A typical PET scanner architecture multichannel ADC is made up of several blocks.By using quick, low-power D flip-flops, most blocks can be constructed. As an alternative solution to this issue, preset-able modified TSPC (MTSPC) D flipflop was suggested. The MTSPC D flip-flop, however, needs one additional PMOS to stop intermediate node toggling.

[30] Seelam Vasavi Sai Viswanada Prabhu Deva Kumar et al., Sequential circuits are logic circuits whose performance depends not only on previous emissions in any event of time. There are two kinds of sequential circuits: I clocked and unlocked. It could be either 1 or 0. These two state circuits are called sequential flip-flops as they state and fall back to another. Sequential circuits are logic circuits whose performance depends not only on previous emissions in any event of time. The easiest sequential circuit sort is a two-state memory cell.

[31] Hardeep Kaur et al., The digital electronics sector was directly targeted at the digital low-power scheme. The use of high-performance computing, wireless communication, consumer electronics, very large-scale integration technology has risen at a very rapid pace. In leakage power consumption, the challenge for VLSI technology is increasing. Wide use of memory storage technologies in modern electronics triggers demand for high efficiency and small area execution of fundamental memory component and D Flip Flop is one of the most state-of - the-art holding elements.

[32] Praveen Kumar chakravarti et al., Due to increased demand for portable devices, low-power device design is now an important field of studies. A single edge initiated D flip flop is suggested in this document with low energy and low area requirements. Using 180 nm

technology, this D flip flop was introduced. D FF's layout is intended using fully automatic, semi-customized layout and customized design methods. From the simulation consequence, it can be noted that the completely custom design showed a 38 percent decrease in region and a 35 percent decrease in energy compared to the fully automatic model. To improve chip density, the general design region is optimized.

[33] Shermina M. Meera et al., Low power dissipation is an important requirement for device design due to increased demand for portable devices. Low-power digital CMOS has become more essential due to improvements in low-power applications, and process technology has been developed. A SET D flip flop with 5 transistors is suggested in this document. Both the dissipation of power and the area were compared.The 5 transistor D FF layout has been designed.From the simulation consequence, it was noted that the fully custom design showed an area decrease of 39 percent and a energy decrease of 37 percent compared to the fully automatic model.With decreased transistor count, this design method achieves the smallest power consumption.

[34] M. Arunlakshman et al., Flip-Flop is an electronic circuit which, in reaction to a clock pulse, stores a logical state of one or more information input signals. During recurring clock intervals to obtain and retain information adequate for other circuits within a scheme to process additional information for a restricted period of time. When the supply voltage is reduced, the velocity of the logic circuits could be reduced owing to the decrease of efficient input voltage for the transistors. The optimum energy-delay-product (EDP) supply voltage for CMOS logic is near to the nMOS transistor Vtn threshold voltage for the real process, provided that the pMOS transistor Vtp threshold voltage is roughly.

[35] P. Prathyusha et al., An significant stream in the design of integrated circuits (IC) is synchronous logic design. In any synchronous design, flip-flops are the fundamental construction blocks. Due to redundant transitions and clocking scheme, a big quantity of energy is consumed by flip flops and latches. Several flip-flops are evaluated using multi-threshold voltage and double-edge triggered clock pair shared flip flops.

Chapter 3

GNRFET

3.1 INTRODUCTION TO GNRFET

Single layered Graphene, ashed composite of carbon, roseasa promising a swer in 2004, considering the way that the primary dimensional surface with hanging advanced, magneto-electronic and optoelectronic properties. Due to extravagant transportability ballistic vehicle, speedy state trading by virtue of especially high administration adaptability and electrostatic decrease in perspective on the 2d structure, Graphene basically based gadget shavea promising future in supplanting standard CMOS nano hardware.

The convenientce of shed Graphene becomes recommended to be 100,000 cm 2V-1s-1 (On protected substrates) and 230,000 cm 2V-1s-1 for suspended structures. Graphene surely

understood a warm conductivity of 5300Wm okay at room temperature. The primary area of Graphene into FET moved toward turning out to be gin 2007. The paper uses Graphene Nano-Ribbon (GNR) FETs. The chance of band opening building in GNR pushes the material for good measured future use in nanoelectronic circuits on account of its recognized qualities which fuse tremendous administration compactness and planar shape. Graphene a two dimensional material is engineered in a honeycomb pearl grid. It has various specific homes. These particular home shave made this material a potential chance for different bundles, for instance electronic gadgets, nanogadgets and dispatch. In any case not withstanding giving superb achievements in fantastic fields, a fundamental disadvantage of zero band holes limits its general execution. Graphene transistors ordinarily called as Graphene FETs display better by and large execution parameters in RF devices and correspondence structures due to its astoundingly high provider mobilities, am bipolarity, high warm conductivity and subsequently outperform the standard Si-based FETs. These transistor devices the use of graphene in like manner are totally used to as the arrangement silicon transistors. In any case, regardless of getting the incredibly extraordinary homes, it encounters its 0band opening.

This zero band gap makes the trading way hard and in like way the on−off extents of those gadgets are nearly nothing. The low on off extent in such gadgets does never again permit turn off and fittingly power wastage happens and results in all things considered execution defilement. The decrease all in all execution defilement can be finished with the guide of building up appropriate band gap in graphene. The outlet of band opening in graphene is finished by methods for different methodologies. Course of action of graphene nano ribbons is one among such method. This is practiced with the guide of encircling parts of graphene by method for decreasing the width of graphene sheet. Decrease in the width of graphene sheet presents band hole right now opening surface as GNRs along the side limits the development of venders and instigate equity hole that is alternately comparative with the width of the ribbon. As width of the ribbon diminishes, the band hole of graphene will increase with the lower. Graphene Nano ribbons are of two sorts. These can be either Zigzag (ZGNRs) or Arm chair(AGNRs).The advanced homes of these graphene nano ribbons can be considered by using the width and the geometry of the GNR along their edges. These additionally have an element desert that is a basic parameter to mull over as the edge flaws prompts for the most part execution shakiness. ZGNRs are steel even as the AGNR are made semiconducting in

nature. Graphene nano ribbons have fundamental bundles in electronic devices containing subject effect transistors.

GNR basically based subject effect transistors is one of the normal transistor dependent on graphene/graphene nano ribbons. Correspondingly a FET, it additionally has the 3 terminals alongside channel, source and the gate. Single layered Graphene, a peeled amalgam of carbon, developed as a promising answer in 2004, as a result of the truth of the key dimensional material with hanging advanced, magneto electronic and optoelectronic properties. By virtue of over the top flexibility ballistic transport, speedy nation changing in view of unfathomably in ordinate administration compactness and electrostatic discount due to the 2d structure,Graphene based completely gadgets have a promising future in supplanting ordinary CMOS nano hardware. The conveyability of peeled Graphene ascend as recommended to be a 100, 000cm 2V-1s-1(On protected substrates) and 230,000cm 2V-1s-1 for suspended structures. Graphene understood a warm conductivity of 5300Wm-1 adequate at room temperature. The basic area of Graphene in to FET progressed toward turning out to be in 2007.

The paper uses Graphene Nano-Ribbon (GNR) FETs. The chance of band void designing in GNR moves the material for sizeable future use in nano-electronic circuits as a result of its undeniable qualities which join colossal provider versatility and planar shape. Graphene a dimensional texture is masterminded in a honeycomb valuable stone grid. Its has various explicit homes. These epic house shave made this material a capacity plausibility for different bundles which fuse electronic gadgets, nano contraptions and discussion.

Any way not withstanding giving wonderful achievements in marvelous fields a straightforward drawback of zero band opening limits its typical execution. Graphene transistors all things considered called as Graphene FETs superstar better quality execution parameters in RF contraptions and correspondence structures due to its strikingly high provider mobilities, ambipolarity, super warm conductivity and in this manner outperform the standard Si-based FETs. These transistor gadgets the usage of graphene moreover are called inlight of the way that the situated up silicon transistors. Regardless, not withstanding

getting the first rate living courses of action, it encounters its zero band opening. This zero band gap makes the trading way hard and thus the on−off extents of these devices are by and pretty much nothing.

The low on off extent in such devices does never again allow get off and in this manner power wastage happens and impacts in all things considered execution defilement. The decrease all things considered display debasement may be finished with the advantage of setting up sensible band opening in graphene. The opening of band hole in graphene is finished by methods for different methodologies. Course of action of graphene nano ribbons is completely one of such methodology. That is accomplished with the benefit of confining parts of graphene through method for diminishing the width of graphene sheet. Refund in the width of graphene sheet presents band hole on this zero band void texture as GNRs along the side limits the development of dealer sand start a force opening it is then again corresponding to the width of the ribbon. As width of the ribbon diminishes, the band hole of graphene will increase with the reduction. Graphene Nano ribbons are of sorts. Those may be both Zigzag(ZGNRs) or Armchair(AGNRs).

The computerized homes of these graphene nano-ribbons may be considered with the guide of the use of the width and the geometry of the GNR close by their edges. Those similarly have include abandons, this is a fundamental parameter to take agandert as the edge deformities prompts ordinary for the most part execution unsteadiness. ZGNRs are metal meanwhile as the AGNR are made semiconducting in nature. Graphene nano-ribbons have noteworthy applications in electronic gadgets including issue sway transistors. GNR based completely issue sway transistors is one of the not odd transistor dependent on graphene/graphene nano-ribbons. In like mannera FET, it besides has the three terminals related to deplete.

3.1.1 INTRINSIC AND EXTRINSIC GRAPHENE

It has one of kind limits, so it's basic to perceive among inward and outward Graphene. Gapless graphene(both mono layer MLG orbilayer BLG) has a charge fairness factor(CNP)

i.e., the Dirac factor, where its character modifications from being electron need to being unfilled individually. see: Density of conditions of graphene is close to the Diracpoint. Any such differentiation isn't important for a2D EG (or BLG with a colossal hole) considering the way that the regular gadget is actually an undoped gadget without an association (and accordingly is dull from the computerized dispatching living courses of action perspective).

In monolayer and bilayer graphene, the ability to gate (or dope) the machine through placing associations in to the conduction or valence band with the guide of tuning an outside gate voltage enables one to pass by methods for the CNP in which the invention limit (EF) is living precisely at the Dirac point. This structure with no loosened venders atT"0", and EF definitely at the Dirac point is all uded to as trademark graphene with a completely packed (empty) valence (conduction) band.

Any minuscule doping (or, for that check, any limited temperature) makes the device extraneous 'with electrons (openings) present inside the conduction (valence) band. Inspite of how the common system is a firm of degree zero (in light of the fact that EF must be unequivocally at the Dirac factor), the dreary testability to tune the contraption from being electron like to being hole like by means of changing over the outside gate voltage, amazingly builds up that one should get moving through the trademark structure at the CNP. If there may be a securing routine in among, as there might be for a gapped structure, by then trademark graphene is n't being gotten as well.

Band structure The band of graphene is very exceptional and the dispersing association E(kx, ky) is addressed with the guide of a cone shaped surface depicted in 2-D equivalent cross-segment [kx,ky]. In addition, being the graphene crosssection framed through two sub-grids An and B as appeared in fig-three, its wave trade mark has two portions and the –electron Hamiltonian in graphene reveals a closeness with the Hamiltonian of mass less.

3.1.2 MATERIAL PROPERTIES OF GRAPHENE

Graphene is a semi metal (zero opening semiconductors) with charge transporters carrying on as massless Dirac fermions. Underneath charge absence of predisposition conditions, theFermi degree is at the square endeavor to the valance and conduction gatherings, yet may be moved with the utilization of a vertical electric controlled order to make a larger piece of openings or electrons. An advancement of the entryway coefficient from practical to horrendous characteristics is resolved. Graphene notable shows incredibly in ordinate provider motility at room temperature because of a vulnerable electron telephone on affiliation. Electrons adventure ballistically in graphene overlong partition (of the solicitation of one micrometer) which for outperform the term of forefront FETs. Graphene is additional than one hundred events more extraordinary than most grounded metal. Mechanical homes of graphene include an exponentially outhful's modulus of ~1TPa and flexible stretch capacity of up to 20%. As structure is altered while graphene is stressed, graphene can be a limit texture for electro-mechanical transducers. Graphene can keep up bleeding edge densities outperforming those of copper at tantamount estimations.

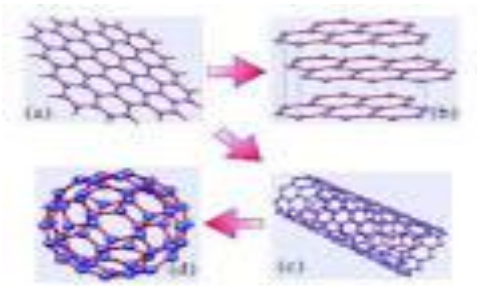

Figure 3.3: Structure of Graphene

3.1.3 HISTORY

One of irrefutably the principal licenses identifying with the formation of graphene recorded in October 2002 entitled, "Nano-scaled Graphene Plates". Following two years, in 2004 Andre Geim and Kostya Novoselov at University of Manchester removed single-particle thick crystallites from mass graphite Geim and Novoselov got a couple of respects for their spearheading ask about on graphene, conspicuously the 2010Nobel Prize in Physics.

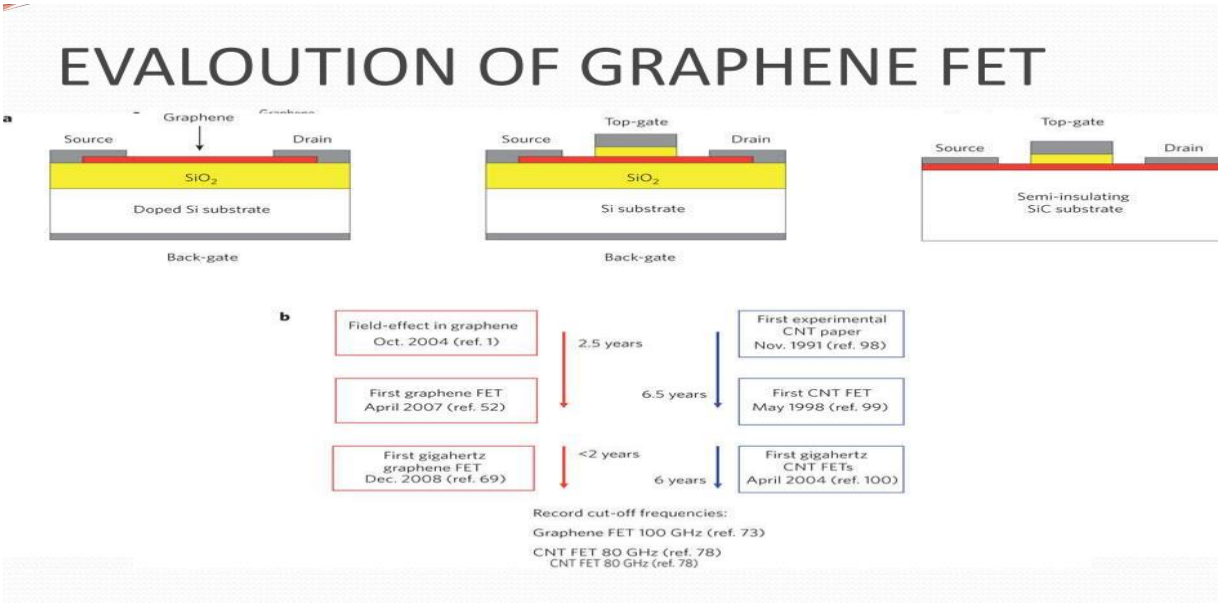

Figure 3.4: Evolution of GrapheneFET

3.2 GNRFET

The graphene nano-ribbon field impact transistor is a developing and forthcoming innovation that showed incredible outcomes in different applications. Late work on GNRFET circuit reenactments has indicated that GNRFETs may have enormous potential in low force applications and design. When reviewed the current work on GNRFET circuit modeling, look at the two assortments of GNRFETs, Metal-Oxide-Semiconducting-(MOS-)type and Schottky-Barrier-(SB-)type GNRFETs, and completely discuss and investigate their separate qualities as far as delay, force, and commotion edge. Starting here of view, we discuss their potential applications, particularly the utilization towards low-power processing.

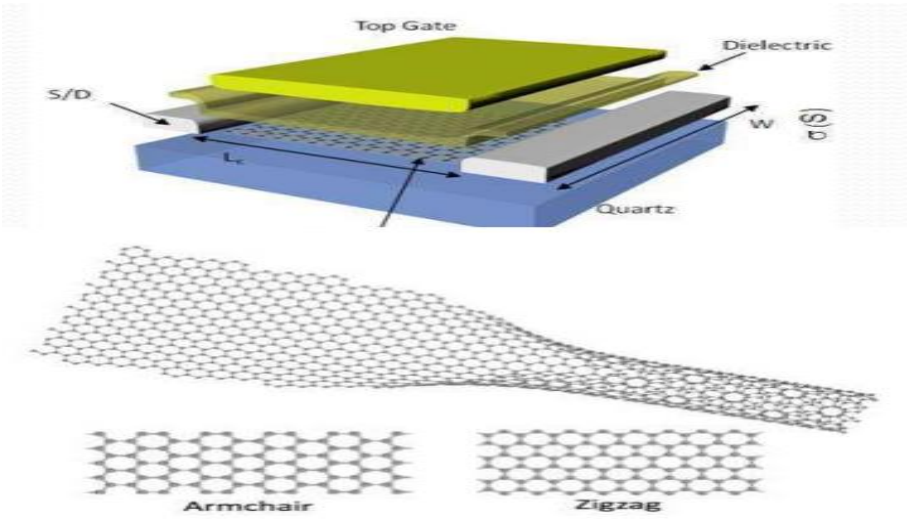

Figure 3.5: GNRFET

Chapter 4

D FLIP FLOP USING MOSFET

4.1 INTRODUCTION

D flip flop's working is a lot of like the D lock aside from that the yield of D Flip Flop takes the condition of the D input right now of a positive edge at the Clock sign (or negative edge if the clock input is dynamic low) and delays it by using one clock cycle. That is the thought process, it's ordinarily referred to as a long at that point flip flop. The D Flip-flop may likewise be interpreted as a delay line or zero order keep up and keep. The capability of the D flip-flop over the D-sort "clear lock" is that the sign on the D input pin is captured the minute the flip-flop is clocked, and subsequent changes on the D information will be overlooked except if the following clock occasion. Right when a circuit is edge triggered the yield can change just on the rising or falling edge of the clock. Be that as it may, by virtue of level-

clocked, the yield can change when the clock is high (or low). In edge enacting yield can change exactly at one minute during the screw cycle; with level timing yield can change during an entire half pattern of the clock. This movement is clearly explained diagrammatically. The fundamental structure or description of DFF and its planning diagram reactions are explained underneath.

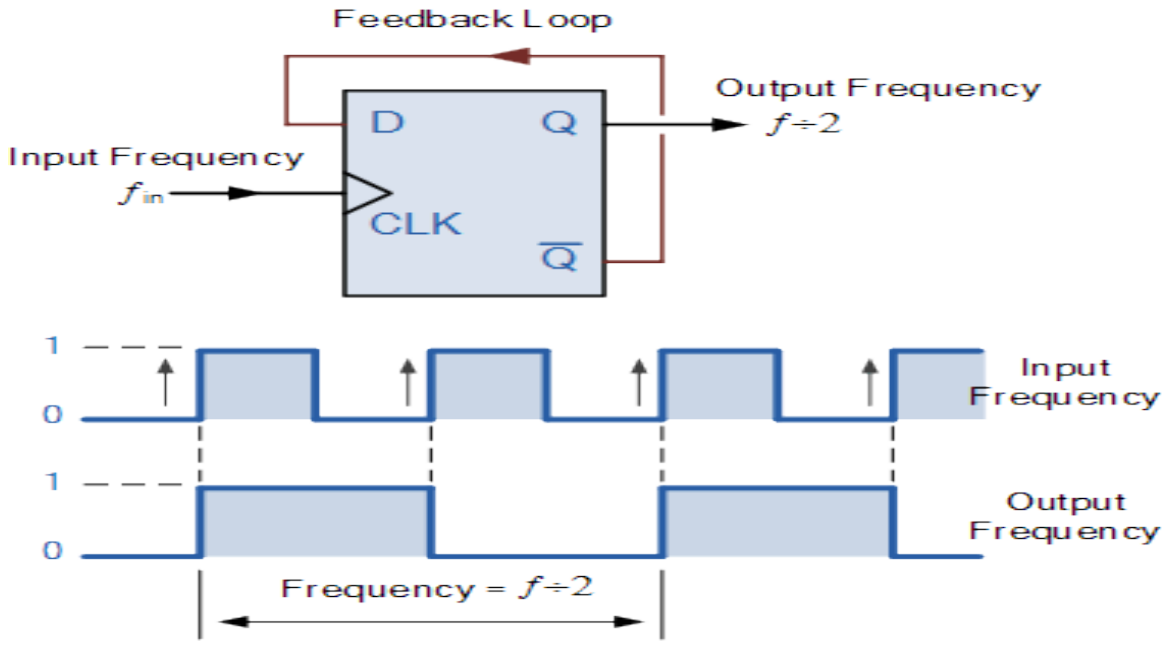

Figure 4.1 Description of D – Flip Flop with its timing diagram

The traditional D – Flip flop is the basic design of DFF. Hooks are consistently called level-touchy considering the way that their yield takes after their contributions as long as they are enabled. They are latent during this whole time when the empower signal is asserted. There are circumstances when it is increasingly helpful to have the yield change just at the rising or falling edge of the empower signal. This empower signal is normally the controlling clock signal. Subsequently, we can have all developments synchronized to the rising or falling edge of the clock. An edge triggered DFF achieves this by participating in course of action a few hooks. The fundamental hook is called the ace lock. The ace lock is enabled when Clk = 0 and takes after the fundamental info D.

When Clk is 1, the ace hook is disabled and slave lock, is enabled with the point that the yield from the ace hook is transferred to the slave hook. The slave lock is enabled while Clk = 1, anyway its substance changes just toward the beginning of the cycle, that is, exactly at the rising edge of the sign because once Clk is 1, the ace hook is disabled and so the contribution

to the slave hook won't change. The traditional DFF made with NAND gates is given underneath. Ordinarily It has four NAND gates totally and an inverter.

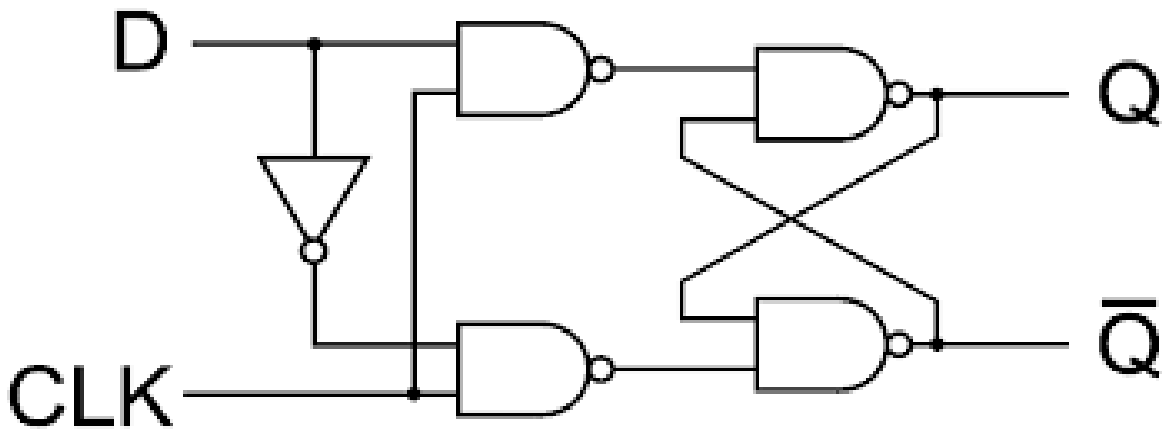

Figure 4.2 D – Flip Flop constructed with NAND gates

Chapter 5
Implementation of TSPC D-Flip Flop using GNRFET in 32nm and 22nm Technology

5.1 GNRFET PARAMETERS AND OUTPUT WAVEFORM

Table 5.1: GNRFET Parameters

Parameter	Description	Value
nRib	The number of GNRs in the device.	2
n	The number of dimer lines in the GNR lattice	6
L	Physical channel length.	32n

Tox	Oxide Thickness between channel and substrate/bottom gate	0.95n
sp	The spacing between the edges of two adjacent GNRs within the same device	3n
dop	Source and Drain reservoirs doping fraction	0.001

Table 5.1 shows the parameters used in coding. The circuits are drawn on paper for giving node diagrams and then implemented through spice coding on Synopsys HSPICE, as HSPICE do not have any schematic maker, this software is used as GNRFET models are compatible with HSPICE.

5.2 IMPLEMENTATION CIRCUITS ON GNRFET

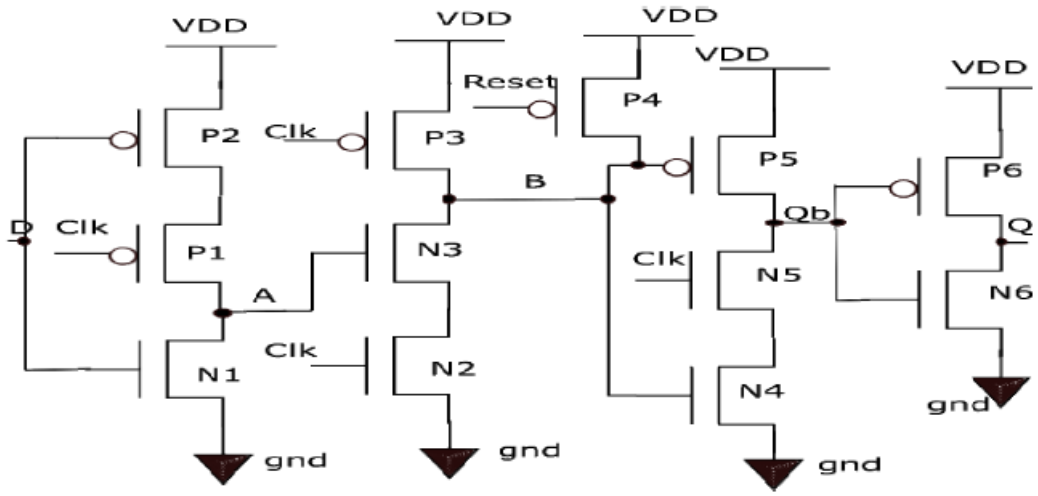

Figure 5.2: TSPC based D Flip Flop

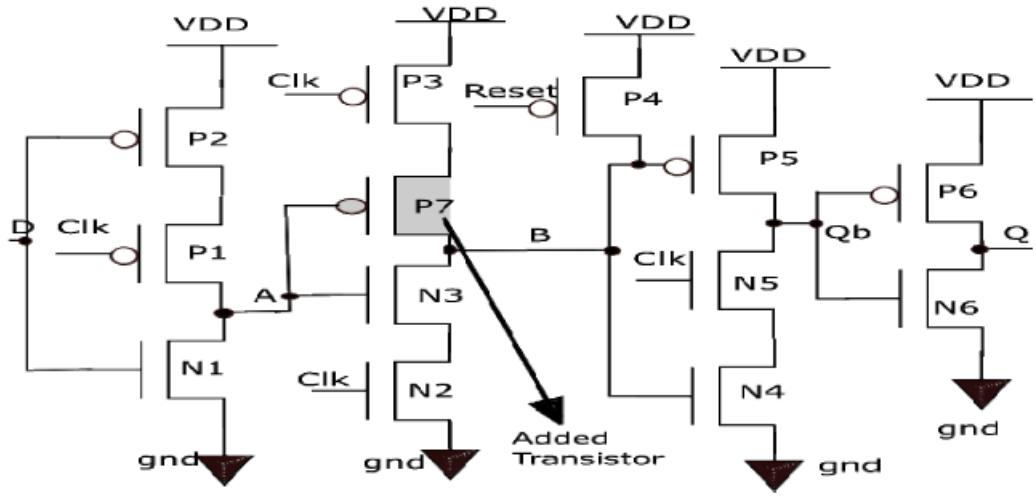

Figure 5.3: Modified TSPC based D Flip Flop

The circuits under consideration for this research work are shown in figure 5.2 and 5.3, as a number of glitches are found in TSPC D flip flop a modified version is also implemented.

5.3 TSPC D FLIP FLOP AND MODIFIED TSPC D FLIP FLOP IN GNRFET

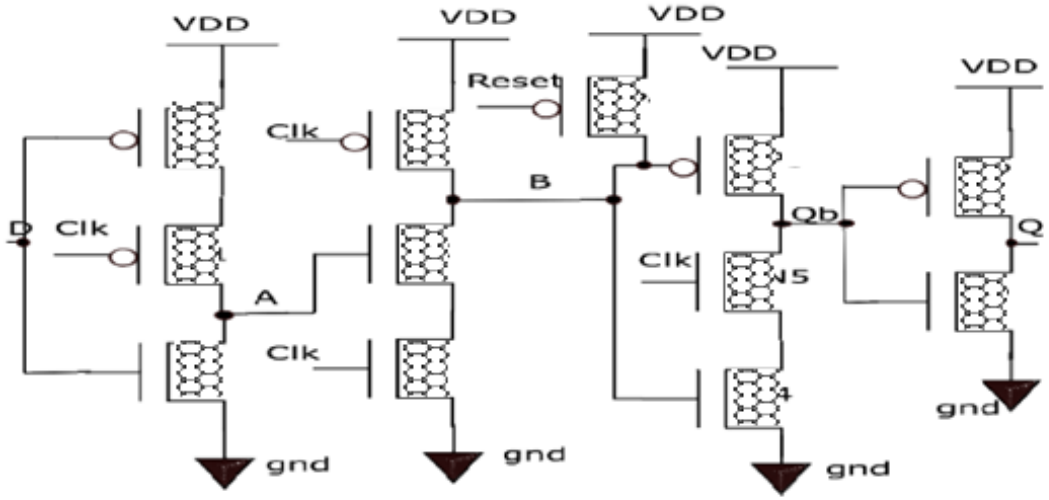

Figure 5.4: TSPC based D Flip Flop GNRFET 22nm

In figure 5.4, the TSPC based DF is implemented using GNRFET in HSPICE through node coding method. Similarly, 5.5 and 5.6 figure are for GNRFET modified and MTCMOS proposed circuit respectively.

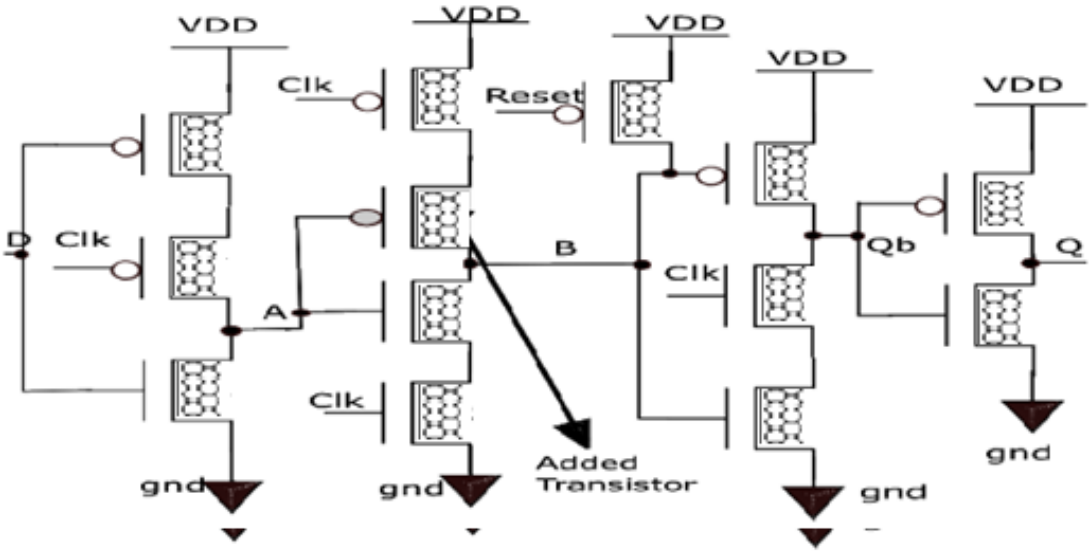

Figure 5.5: Modified TSPC based D Flip Flop GNRFET 22nm

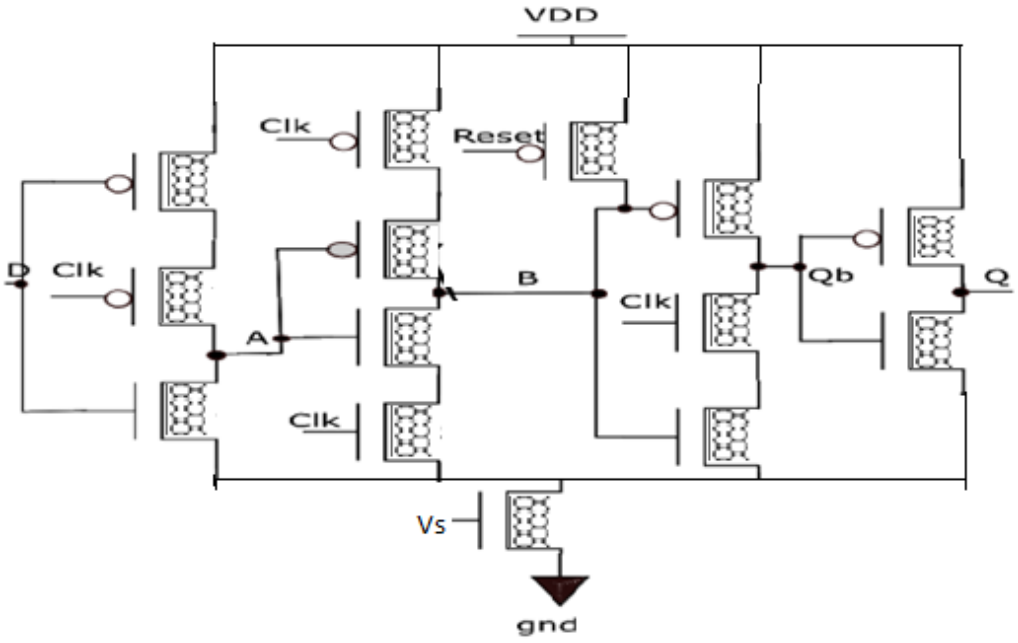

Figure 5.6: Modified TSPC MTCMOS based Proposed D Flip Flop GNRFET 22nm

In the above figure, on ground path a n type GNRFET is added to prevent any leakage path which improves the power and delay in the circuit.

Waveform of TSPCD Flip Flop after GNRFET implementation is shown in Figure 5.7 below.

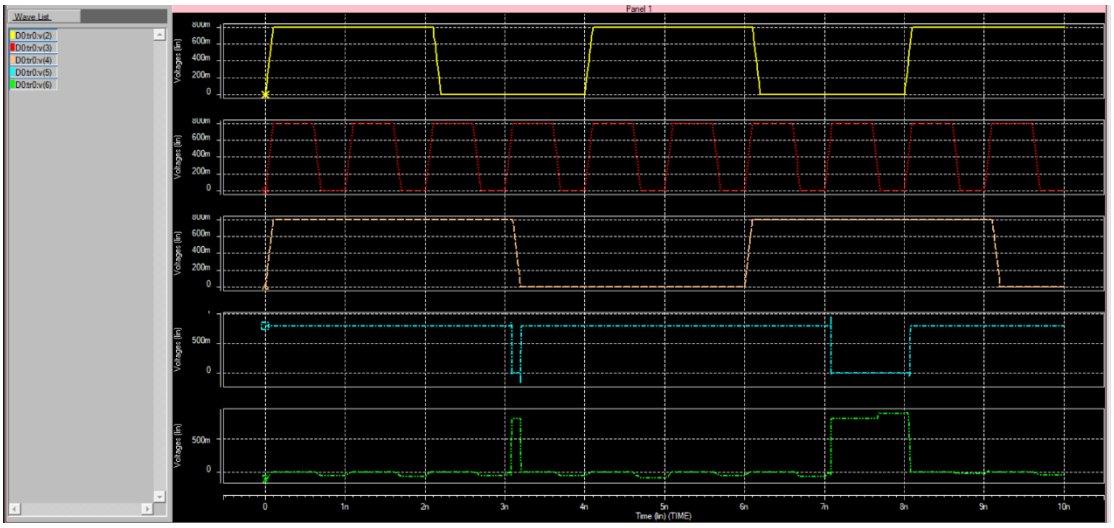

Figure 5.7: Output and Input waveforms for GNRFET based TSPC Circuit

Waveform for GNRFET based 22nm modified and proposed MTCMOS circuit are shown in Figure 5.7 and Figure 5.8.

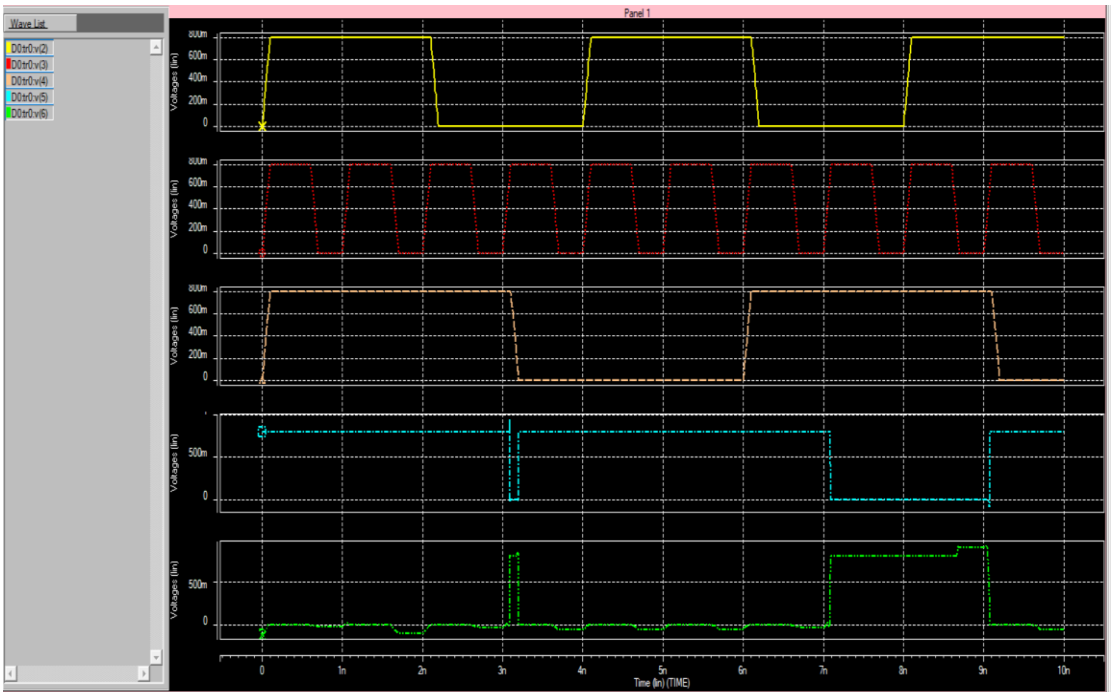

Figure 5.8: Output and Input waveforms for Modified GNRFET based TSPC Circuit

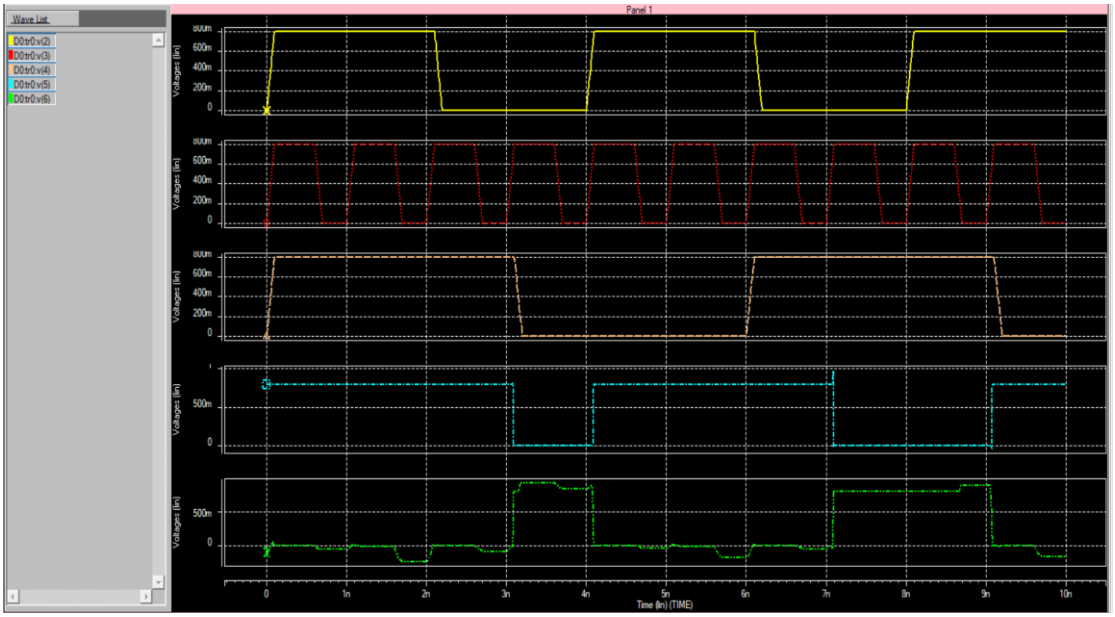

Figure 5.9: Output and Input waveforms for Proposed Modified GNRFET based TSPC Circuit with MTCMOS

In figure 5.9, according to sleep signal VS marked with number 14, gives sleep and active mode for MTCMOS. Also the waveform output comes in accordance with the d input and sleep input, which is main cause of power saving in proposed circuit.

5.4 RESULTS

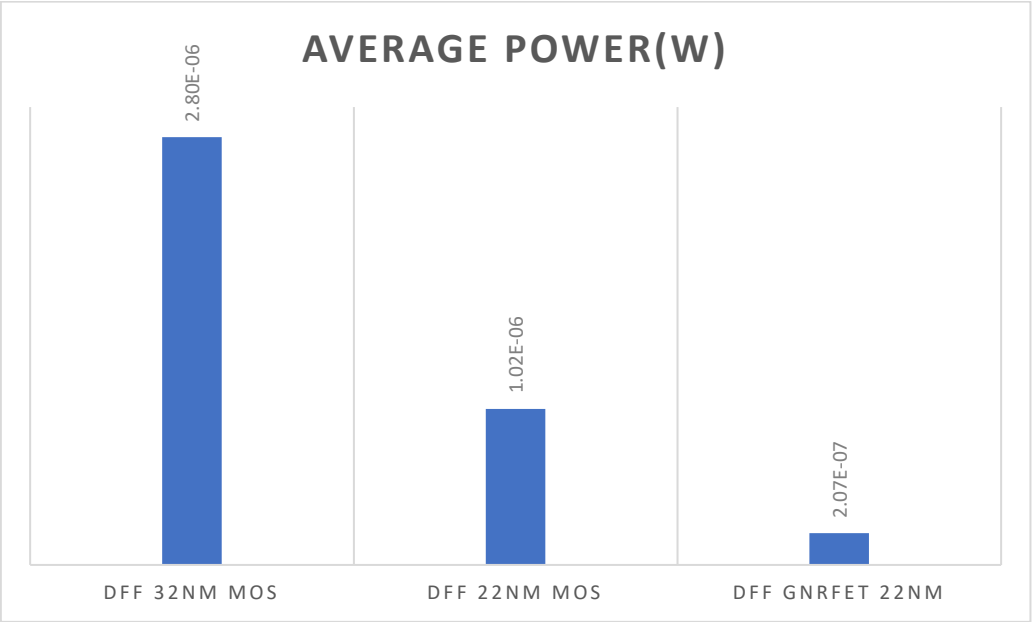

Figure 5.10: Average Power for 32nm and 22nm TSPC DFF MOS and GNR

In figure 5.10, it is seen that average power is lowest in case of TSPC DFF GNR based and highest in 22nm MOS circuit constituting effects of shorter channel.

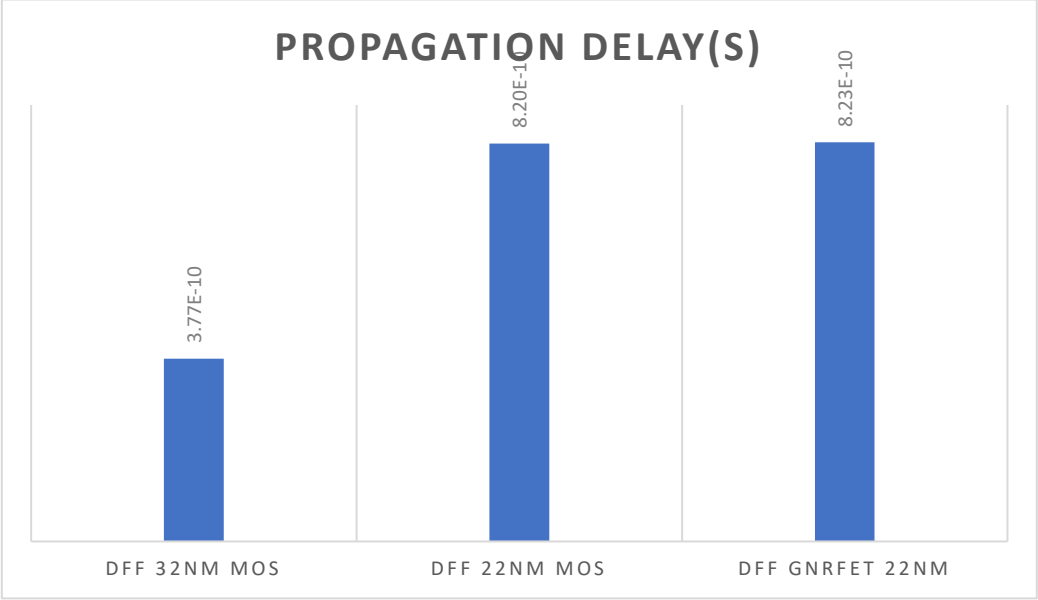

Figure 5.11: Delay for 32nm and 22nm TSPC DFF MOS and GNR

In figure 5.11, similar case for delay is seen as its lowest in GNRFET 22nm based circuit for simple TSPC circuit.

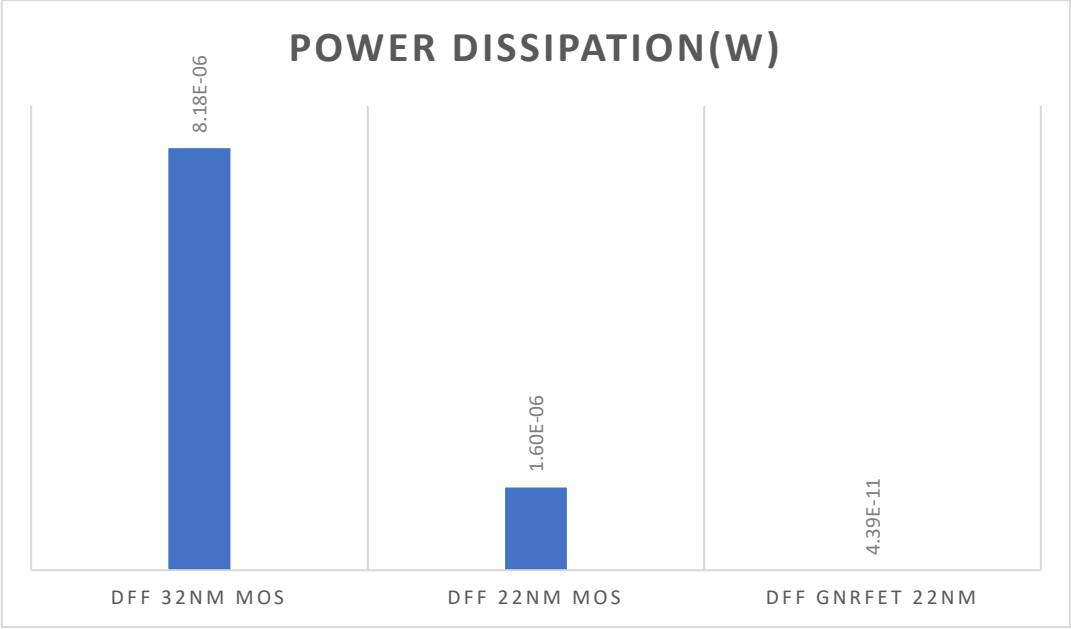

Figure 5.12: Power Dissipation for 32nm and 22nm TSPC DFF MOS and GNR

In figure 5.12 the Power Dissipation is lowest in GNRFET based dynamic TSPC circuit.

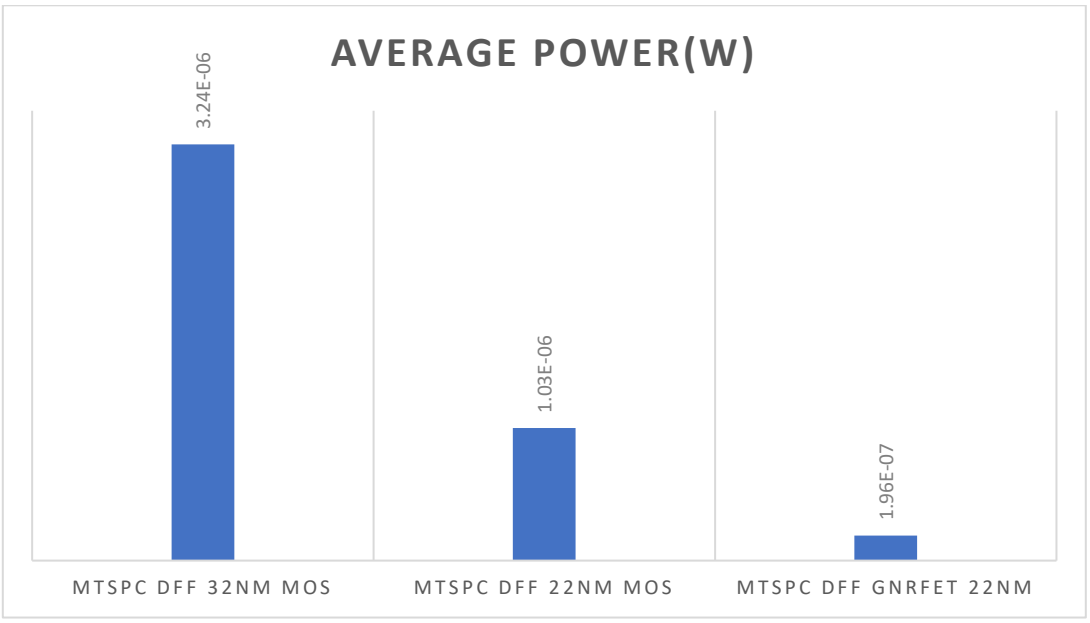

Figure 5.13: Average Power for 32nm and 22nm Modified TSPC DFF MOS and GNR

Similarly, in figure 5.13 and figure 5.14 average power and delay are lowest in case of modified TSPC D flip flop 22nm configuration.

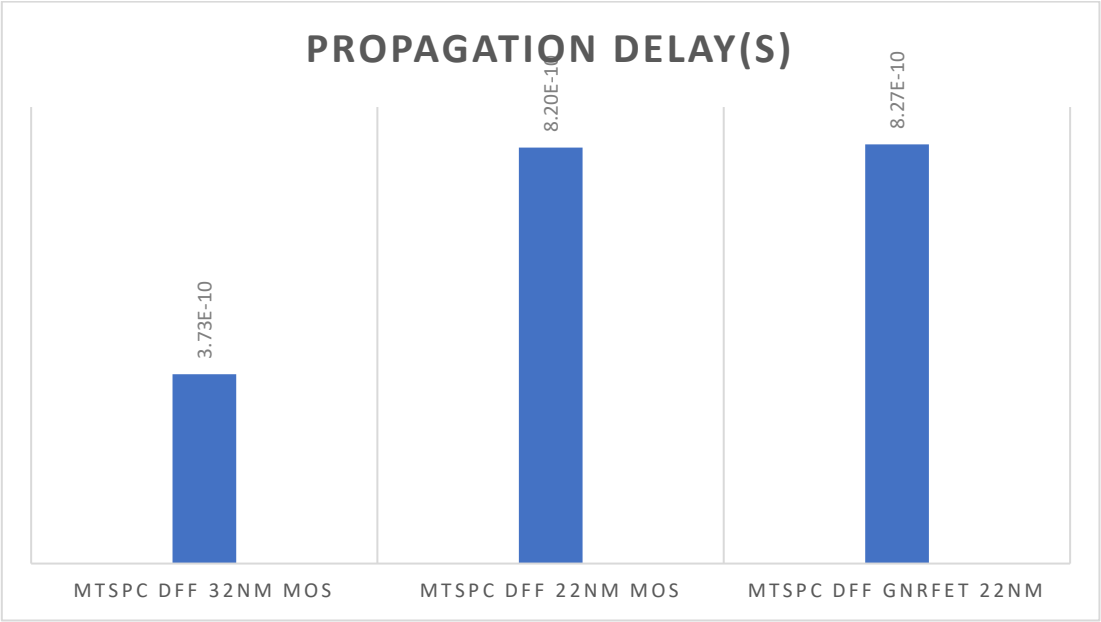

Figure 5.14: Delay for 32nm and 22nm Modified TSPC DFF MOS and GNR

In figure 5.15, the lowest power dissipation is considered in 22nm Modified TSPC DFF.

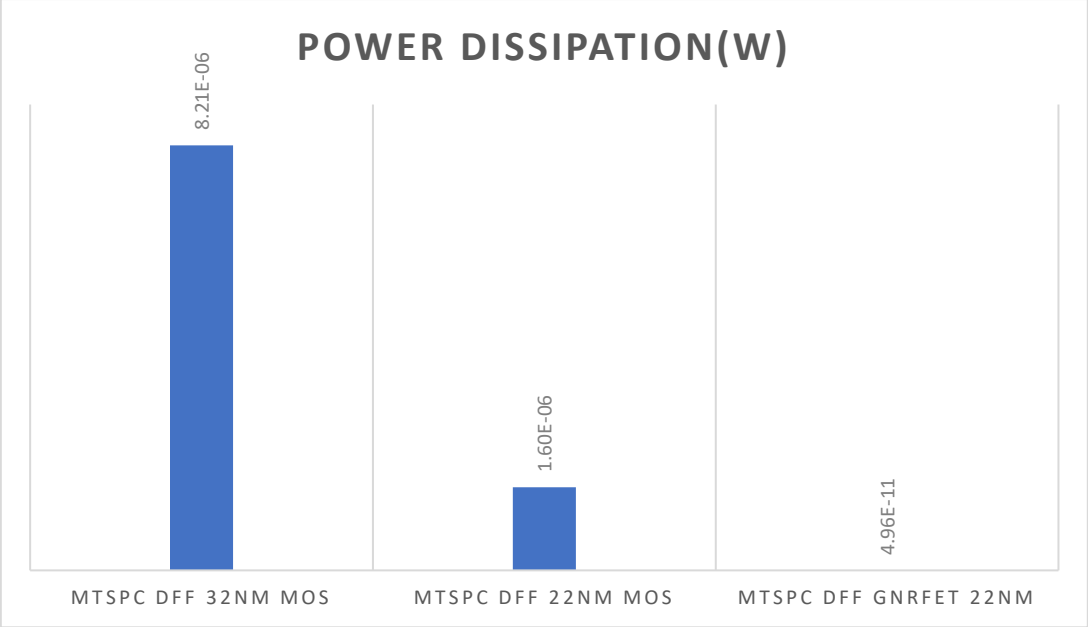

Figure 5.15: Power Dissipation for 32nm and 22nm Modified TSPC DFF MOS and GNR

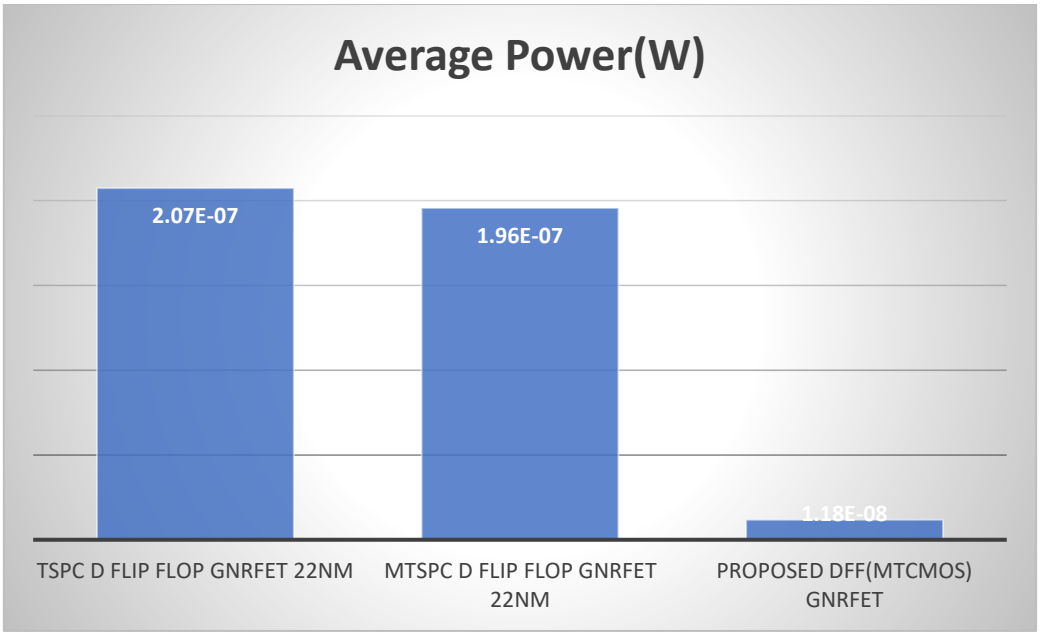

Figure 5.16: Average Power for 32nm and 22nm Proposed MTCMOS based Modified TSPC DFF GNR

In the proposed MTCMOS based modified TSPC D Flip Flop, in figure 5.16 the average power is best, delay is best as in Figure 5.17.

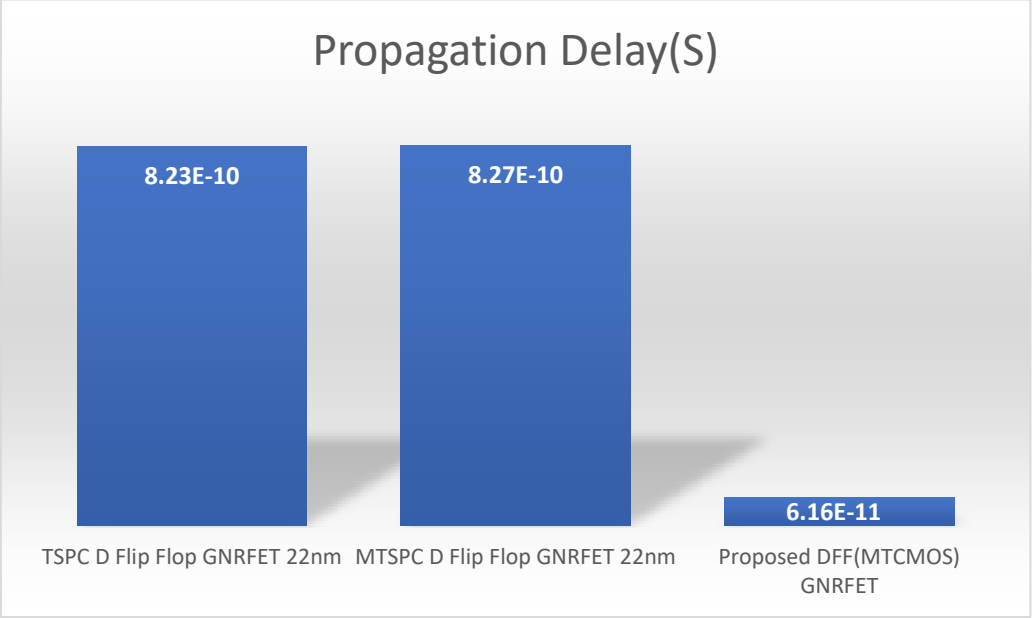

Figure 5.17: Delay for 32nm and 22nm Proposed MTCMOS based Modified TSPC DFF GNR

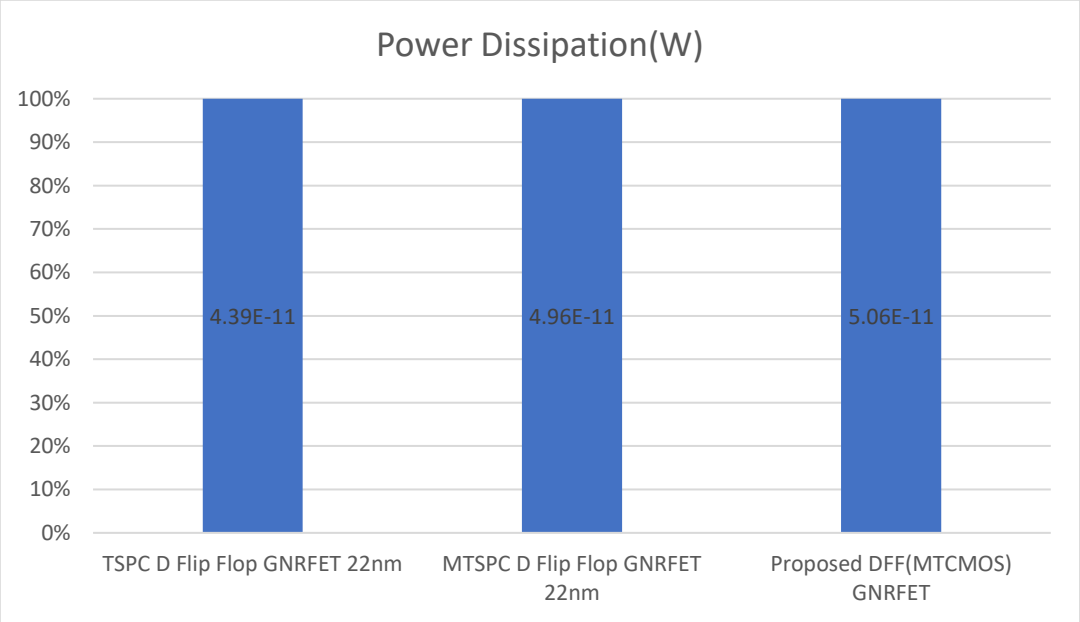

Figure 5.18: Power Dissipation for 32nm and 22nm Proposed MTCMOS based Modified TSPC DFF GNR

As shown in figure 5.18, the Power Dissipation for all GNRFET based circuits are nearly same, which does not give any negative impact on the proposed circuit.

The results in tabular form are shown in table 5.2 and 5.3 below.

Table 5.2: Results in Tabular form for MOS and GNRFET based DFF

	DFF 32nm MOS	**DFF 22nm MOS**	**DFF GNRFET 22nm**
Average Power(W)	2.80E-06	1.02E-06	2.07E-07
Propagation Delay(S)	3.77E-10	8.20E-10	8.23E-10
Power Dissipation(W)	8.18E-06	1.60E-06	4.39E-11
	MTSPC DFF 32nm MOS	**MTSPC DFF 22nm MOS**	**MTSPC DFF GNRFET 22nm**
Average Power(W)	3.24E-06	1.03E-06	1.96E-07
Propagation Delay(S)	3.73E-10	8.20E-10	8.27E-10
Power Dissipation(W)	8.21E-06	1.60E-06	4.96E-11

Table 5.3: Results in Tabular form for GNRFET

	TSPC D Flip Flop GNRFET 22nm	**MTSPC D Flip Flop GNRFET 22nm**	**Proposed DFF(MTCMOS) GNRFET**
Average Power(W)	2.07E-07	1.96E-07	1.18E-08
Propagation Delay(S)	8.23E-10	8.27E-10	6.16E-11
Power Dissipation(W)	4.39E-11	4.96E-11	5.06E-11

Chapter 6
Conclusion and Future Scope

6.1 CONCLUSION

In this thesis, the objectives are fulfilled by proposing a MTCMOS based Dynamic D flip flop which has improved average power and delay. Also by the use of GNRFETs instead of MOS the power dissipation is improved. In 22nm, the short channel effects are reduced by using MOS like GNRFETs. GNRFET ribbon structures promises better low power devices and hence a perfect substitute for the conventional MOS in lower technology length. The average power circuit is improved by 93.9%, propagation delay is improved by 92.5% and power dissipation is nearly same but improved by 99.9% when compared to its MOS counterparts.

6.2 FUTURE SCOPE

On the basis of the work done, these are the following possibilities for future scope:

- It can be further scaled down to 22nm to 16nm technology
- Other parameters like leakage current and noise tolerance can be calculated
- It can be used for low power and high speed ALU applications.
- It will be a promising device for future electronics.
- The circuit will consume less energy because it avoids power consumption in the short circuit.

A new proposed D Flip Flop shows better performance as compared to conventional D Flip Flop. The proposed D Flip Flop can be used for the design of high speed microprocessors as the propagation delay is reduced and hence the operation will be faster and power consumption parameter is also significantly improved significantly.

REFERENCES

[1] Jahangir Shaikh, HafizurRahaman, "High speed and low power preset-able modifie TSPC D flip-flop design and performance comparison with TSPC D flip-flop", *IEEE,* 2018

[2] Naresh Kumar, Umesh Dutta and DileepKumar , "Design of Low Voltage and Low Power D-Flip Flop". *International Journal of Scientific Engineering and Technology*, 2012, www.ijset.com, Volume No.1, Issue No.3, pg : 184-186

[3] Himanshu Kumar, Amresh Kumar, Aminul Islam "Comparative Analysis of D Flip-Flops in Terms of Delay and its Variability" *IEEE*, 2015, pp- 25-37

[4] M.Arunlakshman, "Power and Delay Analysis of DoubleEdge Triggered D-Flip Flop based Shift Registers in 16nm MOSFET Technology*", International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering*, Vol. 3, Issue 4, April 2014, pp-4 to 9

[5] Huei Chaeng Chin,1Cheng Siong Lim,1Weng Soon Wong,1Kumeresan A. Danapalasingam,1Vijay K. Arora,1,2and Michael Loong Peng Tan "Enhanced Device and Circuit-Level PerformanceBenchmarking of Graphene Nano-ribbon Field-Effect Transistoragainst a Nano-MOSFET with Interconnects", *Hindawi Publishing Corporation Journal of Nanomaterials,* Volume 2014, Article ID 879813, 14 pages

[6] N.D. Akhavan, G Jolley, G UmanaMembreno, J Antoszewski, L.Faraone "Study of uniformly doped graphene nano-ribbon transistor (GNR) FET using quantum simulation", *IEEE,* 2012, pp-14-19

[7]Ouyang, Yijian& Yoon, Youngki&Guo, Jing. (2007). Scaling Behaviors of Graphene Nano-ribbon FETs: A Three-Dimensional Quantum Simulation Study. Electron Devices, *IEEE* Transactions on. 54. 2223 - 2231. 10.1109/TED.2007.902692.

[8] Abhijith A Bharadwaj1, Immanuel Keith Soares 2, Madan H R3, H V Ravish Aradhya4 "Design and Performance Comparison of finFET, CNFET and GNRFET based 6T SRAM", *National Conference on Knowledge, Innovation in Technology and Engineering* (NCKITE), 10-11 April 2015

[9] PRAVEENA KUMARI. R, Dr. T.S. JAYADEVA "Design and Analysis of 16bit Ripple Carry Adder and Carry Skip Adder Using Graphene Nano Ribbon Field Effect Transistor (GNRFET)", *International Journal of Innovative Science and Research Technology,* Jul 28, 2017

[10] Sharma, Preetika& Kaur, Inderpreet& Gupta, Shuchi& Singh, Sukhbir. (2016). Effect of temperature on the conductance of GNRFET. 1724. 020075. 10.1063/1.4945195.

[11] Chin, Huei& Lim, Cheng Siong& Soon Wong, Weng& A. Danapalasingam, Kumeresan& K. Arora, Vijay & Tan, Michael. (2014). Enhanced Device and Circuit-Level Performance Benchmarking of Graphene Nano-ribbon Field-Effect Transistor against a Nano-MOSFET with Interconnects. *Journal of Nanomaterials*, 2014. 1-14. 10.1155/2014/879813.

[12] Sanga, MohammadiBanadaki, Yaser& Srivastava, A &Sharifi, Safura. (2016). Graphene nano-ribbon field effect transistor for nanometer-size on-chip temperature sensor. 980203. 10.1117/12.2219346.

[13] Hwang, Wansik& Zhao, Pei & Tahy, Kristof & O. Nyakiti, Luke & D. Wheeler, Virginia & L. Myers-Ward, Rachael & R. Eddy Jr, Charles & Kurt Gaskill, D & Robinson, Joshua &Haensch, Wilfried& An, Huili& , Xing &Seabaugh, Alan & Jena, Debdeep. (2013). Graphene Nano-ribbon Field-Effect Transistors on Wafer-Scale Epitaxial Graphene on SiC substrates. APL Materials. 3. 10.1063/1.4905155.

[14] E. El-hmaily, Hader &Ezz-Eldin, Rabab &Galal, A.I.A. &Hamed, Hesham. (2018). High Performance GNR MTCMOS for Low-Voltage CMOS Circuits.

[15] M. Akbari Eshkalak "Graphene Nano-Ribbon Field Effect Transistor underDifferent Ambient Temperatures*", Iranian Journal of Electrical & Electronic Engineering*, Vol. 12, No. 2, June 2016

[16] Yoon, Youngki& Fiori, Gianluca& Hong, Seokmin&Iannaccone, Giuseppe &Guo, Jing. (2008). Performance Comparison of Graphene Nano-ribbon FETs With Schottky Contacts and Doped Reservoirs. *IEEE Transactions on Electron Devices*, 55. 10.1109/TED.2008.928021.

[17] Mayank Mishra, RonilStieven Singh ,Ale Imran "Performance optimization of GNRFET Inverter at 32nm technology node", *materials today proceeding*, Volume 4, Issue 9, 2017, Pages 10607-10611

[18] DEVENDRA UPADHYAY and SUDHANSHU CHOUDHARY "Understanding the impact of graphene sheet tailoring on theconductance of GNRFETs", *Bull. Mater. Sci*., Vol. 38, No. 7, December 2015, pp. 1705–1709.c©Indian Academy of Sciences.

[19] Maedeh Akbari Eshkalaka,n, Rahim Faezb, Saeed Haji-Nasiria "A novel graphene nano-ribbonfield effect transistor with two differentgate insulators" http://dx.doi.org/10.1016/j.physe.2014.10.0211386-9477/&2014 Elsevier

[20] DehdashtiAkhavan, Nima&Ferain, Isabelle & Yu, Ran &Razavi, Pedram&Colinge, Jean-Pierre. (2012). Influence of discrete dopant on quantum transport in silicon nanowire transistors. *Solid State Electronics*. 70. 92-100. 10.1016/j.sse.2011.11.017.

[21] Choudhury, Mihir& Yoon, Youngki&Guo, Jing &Mohanram, Kartik. (2008). Technology exploration for graphene nano-ribbon FETs. 272-277. 10.1145/1391469.1391539.

[22] Yousefi, Reza &Ghoreishi, Seyed. (2017). A computational study of a novel graphene nano-ribbon field effect transistor Read More: http://www.worldscientific.com/doi/abs/10.1142/S0217979217500564?src=recsys.
International Journal of Modern Physics B. 10.1142/S0217979217500564.

[23] M.Arunlakshman "Effect of 15nm Graphene Nano Ribbon Field Effect Transistors(GNRFET)on Single Edge Triggered D –Flip Flop based Shift Registers and its comparison with 16nm MOSFET Technology", *International Journal of Emerging Technology and Advanced Engineering* Website: www.ijetae.com(ISSN 2250-2459,ISO 9001:2008Certified Journal,Volume 4, Issue 4,April2014),

[24] Wan Sik Hwang1,2,b), Pei Zhao1, Kristof Tahy1, Luke O. Nyakiti3,4, Virginia D. Wheeler3, Rachael L. Myers-Ward3, Charles R. Eddy Jr.3, D. Kurt Gaskill3, Joshua A. Robinson5, Wilfried Haensch6, Huili (Grace) Xing1, Alan Seabaugh1, and Debdeep Jena1,b)"Graphene nano-ribbon field-effect transistors on wafer-scale epitaxial graphene on SiC substrates" *APL Materials* 3, 011101 (2015); https://doi.org/10.1063/1.4905155

[25] M. M. Anas, "A Study of Single Layer and Bilayer GNRFET," *2016 UKSim-AMSS 18th International Conference on Computer Modelling and Simulation (UKSim),* Cambridge, 2016, pp.93-96.doi: 10.1109/UKSim.2016.50

[26] Mr. Prathamesh G. Dhoble Mr. Avinash D. Kale "Design High Speed Conventional D Flip-Flop using 32nm CMOS Technology "IJIRST –International Journal for Innovative Research in Science & Technology| Volume 1 | Issue 11 | April 2015 ISSN (online): 2349-6010

[27] Ms. Chaitali V. Matey, Ms. Shraddha K. Mendhe , Mr. Sandip A. Zade "A Novel Design Of Counter Using Tspc D Flip-Flop For High Performance And Low Power Vlsi Design Applications Using 45nm Cmos Technology "International Journal of Science Technology & Management Volume No.04, Special Issue No.01, February 2015 ISSN (Print) 2394-1529, (Online) 2394-1537

[28] Prathamesh G. Dhoble, Avinash D. Kale "Design of Positive Edge Triggered D Flip-Flop Using 32nm CMOS Technology" International Standards Organization Vol. 3, Issue 4, April 2015

[29] Jahangir Shaikh, Hafizur Rahaman "High speed and low power preset-able modified TSPC D flip-flop design and performance comparison with TSPC D flip-flop" IEEE transactions on very large scale integrated circuits(VLSI) systems, vol.10, no.5, October 2002

[30] Seelam Vasavi Sai Viswanada Prabhu Deva Kumar "Implementation Of Low Powerd D Flipflop Using 45nm Cmos Technology" Journal of Recent Scientific Research 8, Issue, 6, pp. 17729-17732, June, 2017

[31] Hardeep Kaur, Er.Swarnjeet Singh, Sukhdeep Kaur "Design and Analysis of D Flip Flop Using Different Technologies" International Journal of Innovative Research in Computer and Communication Engineering (An ISO 3297: 2007 Certified Organization) Vol. 3, Issue 7, July 2015

[32] Praveen Kumar chakravarti , Rajesh Mehra “Layout design of D Flip Flop for Power and Area Reduction” International Journal of Scientific Research Engineering & Technology (IJSRET) ISSN: 2278–0882 EATHD-2015 Conference Proceeding, 14-15 March, 2015

[33] Shermina M. Meera , Shahanaz M. Meera , Nishi G. Nampoothiri “Layout Design of 5 Transistor D Flip Flop for Power and Area Reduction and Performance Comparison in Different Scaling Technologies “International Standard Serial Number (**ISSN**) ,2018 (Volume 4, Issue 1)

[34] M.Arunlakshman “Power and Delay Analysis of Double Edge Triggered D-Flip Flop based Shift Registers in 16nm MOSFET Technology” International Organization for Standardization Vol. 3, Issue 4, April 2014

[35] P. Prathyusha , G. Mary Sowjanya “Design of High Performance Double Edge Triggered D-Flip flop using MTCMOS Technique” (An ISO 3297: 2007 Certified Organization) Vol. 4, Issue 7, July 2015

APPENDIX A

SPICE MODEL

BASIC SPICE COMMANDS

Voltage source: The command will start with v to defining the voltage source and we are using two types of voltage source DC and PULSE

DC SOURCE

SYNTAX: Vname N+ N- <DC > Value

Where: Vname is the name of voltage source
DC for defining the source as dc source
N+ is the positive terminal
N– is the negative terminal

Example: VVoltageSource_1 VddGnd DC 1.0

PULSE SOURCE

SYNTAX: Vname N+ N- PULSE(Vo V1 Td TrTf Tw To)

Where: Vname is the name of voltage source
N+ is positive terminal
N- is ground terminal
PULSE is the type of voltage source
Vo is initial voltage
V1 is final voltage
Td is initial delay time
Tr is rise time
Tf is fall time
Tw is pulse width
To is period of wave

Example: VVoltageSource_2 clkGnd PULSE(0 1.0 0n 5n 05n 30n 100n)

.include

This statement is use to include the file or subciruits in the current circuit.

SYNTAX: .include 'filename'

Where: ‘filename’ is the path of the file

.lib

To create and read from libraries of commonly-used commands, device models, subcircuit analysis, and stat ements in library files, use the.LIB call statement. As HSPICE or HSPICE RF encounters each .LIB call name in the main data file, it reads the corresponding entry from the designated library file, until it finds an .ENDL statement.

SYNTAX: .lib 'filename'

Where: 'filename' is the path of the file

.TRAN Statement

This statement specifies the time interval over which the transient analysis takes place, and the time increments. The format is as follows:

SYNTAX: .TRAN TSTEP TSTOP <TSTART <TMAX>><UIC>

Where: TSTEP is the printing increment.

TSTOP is the final time

TSTART is the starting time (if omitted, TSTART is assumed to be zero)

TMAX is the maximum step size

UIC stands for Use Initial Condition and instructs HSPICE not to do the quiescent operating point before beginning the transient analysis. If UIC is specified, HSPICE will use the initial conditions specified in the element statements.

.PRINT and .PLOT

These statements will instruct HSPICE what output to generate. If you do not specify an

output statement, HSpice will always calculate the DC operating points. The two types of

outputs are the .PRINTs and .PLOTs . A print is a table of data points and a plot is a
low-resolution graphical representation.

SYNTAX: .PRINT TYPE OV1 OV2 OV3
.PLOT TYPE OV1 OV2 OV3

in which TYPE specifies the type of analysis to be printed or plotted and can be DC,
TRAN or AC.

The output variables are OV1, OV2 and can be voltage between nodes, the voltage between a node and ground. With currents, you can also specify the currents between
nodes and more importantly, the currents running through a particular voltage source, which is useful for power consumption. In addition, you can define the type of output by
simply putting a suffix after V or I. The suffixes are:

- M: Magnitude
- DB: Magnitude in dB (deciBels)
- P: Phase
- R: Real part
- I: Imaginary part

.MEASURE

.MEASURE is often used in circuit optimization. With it, you can find when a certain event occurs as you sweep various parameters. You can use .MEASURE for finding:

- Rise ,Fall and Time Delay
- Average, RMS, min, max, peak-to-peak and integral
- Find X when Y occurs
- Derivative and Integral Evaluation
- Equation Evaluations

.END

the end statement of the circuit is always be .END. This statement must be a line by itself, followed by a carriage return!