GALGOTIAS UNIVERSITY

(Established under Galgotias University Uttar Pradesh Act No. 14 of 2011)

# School of Electrical, Electronics and Communication Engineering

## Program: M. Tech VLSI Design

Scheme: 2017/2018/2019

## Curriculum

### Semester 1

| Sl. No | Course Code | Name of the Course | | | | | Assessment Pattern | | |
|---|---|---|---|---|---|---|---|---|---|
| | | | L | T | P | C | IA | MTE | ETE |
| 1 | MATH5001 | Advanced Numerical & Statistical Methods | 3 | 1 | 0 | 4 | 20 | 30 | 50 |
| 2 | MVLS5020 | Advanced Digital System Design | 3 | 0 | 0 | 3 | 20 | 30 | 50 |
| 3 | MVLS5021 | Advanced VLSI Design | 3 | 0 | 0 | 3 | 20 | 30 | 50 |
| 4 | MVLS5004 | Analog Filter Design | 3 | 0 | 0 | 3 | 20 | 30 | 50 |
| 5 | MVLS**** | Program Elective 1 | 3 | 0 | 0 | 3 | 20 | 30 | 50 |
| 6 | MVLS5019 | Advanced Digital System Design Lab | 0 | 0 | 2 | 1 | 50 | - | 50 |
| 7 | MVLS5022 | Advance VLSI Design Lab | 0 | 0 | 2 | 1 | 50 | - | 50 |
| | | **Total** | **15** | **1** | **4** | **18** | | | |

### Semester II

| Sl No | Course Code | Name of the Course | | | | | Assessment Pattern | | |
|---|---|---|---|---|---|---|---|---|---|
| | | | L | T | P | C | IA | MTE | ETE |
| 1 | CENG5001 | Professional and Communication skills | 0 | 0 | 4 | 2 | 20 | 30 | 50 |
| 2 | MVLS5007 | DSP for VLSI | 3 | 0 | 0 | 3 | 20 | 30 | 50 |
| 3 | MVLS5008 | VLSI Testing and fault Tolerance | 3 | 0 | 0 | 3 | 20 | 30 | 50 |
| 4 | MVLS5009 | ASIC Design and FPGAs | 3 | 0 | 0 | 3 | 20 | 30 | 50 |
| 5 | MVLS**** | Program Elective 2 | 3 | 0 | 0 | 3 | 20 | 30 | 50 |
| 6 | MVLS**** | Program Elective 3 | 3 | 0 | 0 | 3 | 20 | 30 | 50 |
| 7 | MVLS5012 | ASIC Design Lab | 0 | 0 | 2 | 1 | 50 | - | 50 |
| 8 | MVLS5013 | DSP for VLSI Lab | 0 | 0 | 2 | 1 | 50 | - | 50 |
| | | **Total** | **15** | **0** | **8** | **19** | | | |

### Semester III

| Sl No | Course Code | Name of the Course | | | | | Assessment Pattern | | |
|---|---|---|---|---|---|---|---|---|---|
| | | | L | T | P | C | IA | MTE | ETE |
| 1 | MVLS6001 | Embedded System Design | 3 | 0 | 0 | 3 | 20 | 30 | 50 |
| 2 | MVLS**** | Program Elective 4 | 3 | 0 | 0 | 3 | 20 | 30 | 50 |
| 3 | MVLS**** | Program Elective 5 | 3 | 0 | 0 | 3 | 20 | 30 | 50 |
| 4 | MVLS6004 | Embedded System Lab | 0 | 0 | 2 | 1 | 50 | - | 50 |
| 5 | MVLS9997 | Research Seminar | 0 | 0 | 2 | 1 | 50 | - | 50 |
| 6 | MVLS9998 | Capstone Design- 1 | 0 | 0 | 10 | 5 | 50 | - | 50 |
| | | **Total** | **9** | **0** | **14** | **16** | | | |

### Semester IV

| Sl No | Course Code | Name of the Course | | | | | Assessment Pattern | | |
|---|---|---|---|---|---|---|---|---|---|
| | | | L | T | P | C | IA | MTE | ETE |
| 1 | MVLS9999 | Capstone Design- 2 | 0 | 0 | 30 | 15 | 50 | - | 50 |
| | | **Total** | **0** | **0** | **30** | **15** | | | |

**Programme Elective**

| Sl. No. | Course Code | Course Title | L | T | P | C |
|---|---|---|---|---|---|---|
| 1 | MVLS5003 | Advanced VLSI Technology | 3 | 0 | 0 | 3 |
| 2 | MVLS5005 | MOS Device Modelling | 3 | 0 | 0 | 3 |
| 3 | MVLS5010 | Advanced Digital VLSI Design | 3 | 0 | 0 | 3 |
| 3 | MVLS5011 | Low power VLSI Design | 3 | 0 | 0 | 3 |
| 4 | MVLS5014 | Sensor Technology and MEMS | 3 | 0 | 0 | 3 |
| 7 | MVLS5015 | Nano-Electronics | 3 | 0 | 0 | 3 |
| 8 | MVLS5016 | Design of Semiconductor Memories | 3 | 0 | 0 | 3 |
| 9 | MVLS5017 | Advanced Analog VLSI Design | 3 | 0 | 0 | 3 |
| 10 | MVLS5018 | Reconfigurable Computing | 3 | 0 | 0 | 3 |
| 11 | MVLS6002 | Physical Design Automation | 3 | 0 | 0 | 3 |
| 12 | MVLS6003 | System-on-Chip Design | 3 | 0 | 0 | 3 |
| 13 | MVLS6005 | Packaging and Interconnect Analysis | 3 | 0 | 0 | 3 |
| 14 | MVLS6006 | EMI and EMC in System Design | 3 | 0 | 0 | 3 |
| 15 | MVLS6007 | DSP Architecture | 3 | 0 | 0 | 3 |
| 16 | MVLS6008 | Mixed Signal IC Design | 3 | 0 | 0 | 3 |

# Detailed Syllabus

| Name of The Course | Advanced Numerical & Statistical Methods | | | |
|---|---|---|---|---|
| Course Code | MATH5001 | | | |
| Prerequisite | Matrices and Calculus | | | |
| | L | T | P | C |
| | 3 | 1 | 0 | 4 |

**Course Objectives:** To introduce the applications and trade off of various advanced methods used to solve a wide variety of engineering problems dealing with algebraic and differential equation that are often encountered in engineering and cannot be solved by analytical methods along with the introduction of design of experiment.

**Course Outcomes**

| | |
|---|---|
| **CO1** | Do numerical integration for various problems |
| **CO2** | Do interpolation using various interpolation techniques. |
| **CO3** | Understand the Ordinary & Partial Differential equations and their solutions. |
| **CO4** | Do numerical integration |
| **CO5** | Use wavelets and their applications |

**Text Book (s)**

1. **Numerical Method** : E. Balagurusamy , Tata McGraw Hill Publication.
2. **Applied Numerical Analysis :** Curtis F. Gerald and Patrick O. Wheatley – Pearson Education Ltd.

**Reference Book (s)**

1. **Numerical Methods for Scientific and Engineering computation:** M.K Jain, S.R.K Iyengar and R.K Jain, New age International Publishers.
2. **Statistical Methods :** S.P. Gupta, Sultan Chand and Sons
3. **Introduction to Mathematical Statistics:** A.M. Mood, F. Graybil and D.C.Boes, Mc Graw Hill Publication.

**Course Content:**

| **Unit-1** | **System of Equations** | **8 hours** |
|---|---|---|
| Solution of system of linear equations- Direct Methods- Gauss elimination – Pivoting, Partial and Total Pivoting, Triangular factorization method using Crout LU decomposition, Cholesky method, Iterative Method- Gauss-Seidel and Jacobi method, ill conditioned matrix<br>Solution of system of non linear equation- Newton Raphson and Modified Newton Raphson Method. Iterative methods. | | |
| **Unit-2** | **Interpolation and Approximation** | **8 hours** |
| Lagrange, Spline and Hermite interpolation, Approximations, Error of approximation, Norms for discrete and continuous data, Least square approximation. | | |
| **Unit-3** | **Numerical Integration** | **8 hours** |
| Newton Cotes closed Quadrature, Gauss Legendre Quadrature, Multiple Integration. | | |
| **Unit-4** | **Numerical Solution of Differential Equations** | **8 hours** |
| Finite Difference Schemes, Numerical solution of Ordinary differential equation using Modified Euler's method, Runge-Kutta method of 2nd, 3rd and 4th orders, Predictor- Corrector method, Solution of Laplace's and Poisson's equations by Liebmann's method, Solution of one dimensional time dependent heat flow. | | |

| Unit-5 | Probability and statistics | 8 hours |
|---|---|---|
| Review of concept of probability, Random Variables, Continuous and discrete distribution function, moments and moments generating functions, Binomial, Poisson, Negative Binomial, Geometric and Hyper-geometric Distributions, Uniform, Normal, Exponential, Gamma and Beta distributions. Point and Interval estimation, Testing of Hypothesis (t-test and chi square test), Analysis of variance and Introduction of Design of experiments. | | |

**Continuous Assessment Pattern**

| Internal Assessment (IA) | Mid Term Test (MTE) | End Term Test (ETE) | Total Marks |
|---|---|---|---|
| 20 | 30 | 50 | 100 |

| Name of The Course | Advanced Digital System Design | | | |
|---|---|---|---|---|
| **Course Code** | **MVLS5020** | | | |
| **Prerequisite** | Digital Electronics | | | |
| | **L** | **T** | **P** | **C** |
| | 3 | 0 | 0 | 3 |

**Course Objectives:**.

This course describes about the logic design techniques using simple combinational and sequential circuits to FPGAs, CPLDs.

**Course Outcomes**

| | |
|---|---|
| **CO1** | Understand the Basics of MOS transistor Theory |
| **CO2** | Understand the Device Modeling techniques using CAD and analyze the parameters which degrades the functionality of MOS Devices |
| **CO3** | Design Complex CMOS Circuits |
| **CO4** | Understand and design various combinational and Sequential Circuits using CMOS Transistors |
| **CO5** | Perform Data Path Operations using CMOS Circuits |

**Text Book (s):**


1. T.R. Padmanabhan, B Bala Tripura Sundari, Design Through Verilog HDL, Wiley 2009.
2. Zainalabdien Navabi, Verliog Digital System Design,TMH, 2nd Edition.
3. Fundamentals ofDigital Logic with Verilog Design - Stephen Brown,Zvonkoc Vranesic, TMH, 2nd Edition.


**Reference Book (s)**


1. Advanced Digital Logic Design using Verilog, State Machines & Synthesis for FPGA - Sunggu Lee, Cengage Learning, 2012.
2. Verilog HDL - Samir Palnitkar, 2nd Edition, Pearson Education, 2009.
3. Advanced Digital Design with Verilog HDL - Michel D. Ciletti, PHI,2009.


**Course Content:**

| **Unit-1** | **Overview of Verilog HDL** | **10 hours** |
|---|---|---|
| **Introduction to VerilLog HDL:** Verilog as HDL, Levels of Design Description, Concurrency, Simulation and Synthesis, Function Verification, System Tasks, Programming Language Interface, Module, Simulation and Synthesis Tools<br>**Language Constructs and Conventions:** Introduction, Keywords, Identifiers, White Space, Characters, Comments, Numbers, Strings, Logic Values, Strengths, Data Types, Scalars and Vectors, Parameters, Operators. | | |
| **Unit-2** | **Modeling Concepts -I** | **8 hours** |
| **Gate Level Modeling:** Introduction, AND Gate Primitive, Module Structure, Other Gate Primitives, Illustrative Examples, Tristate Gates, Array of Instances of Primitives, Design of Flip-Flops with Gate Primitives, Delay, Strengths and Construction Resolution, Net Types, Design of Basic Circuit. | | |

| | | |
|---|---|---|
| **Modeling at Dataflow Level:** Introduction, Continuous Assignment Structure, Delays and Continuous Assignments, Assignment to Vector, Operators. | | |
| **Unit-3** | **Modeling Concepts -II** | **8 hours** |
| **Behavioural Modeling:** Introduction, Operations and Assignments, Functional Bi furcation, 'Initial' Construct, Assignments with Delays, 'Wait Construct, Multiple Always Block, Designs at Behavioural Level, Blocking and Non-Blocking Assignments, The 'Case' Statement, Simulation Flow, 'If' an 'if-Else' Constructs, 'Assign- De-Assign' Constructs, 'Repeat' Construct, for loop, 'The Disable' Construct, 'While Loop', Forever Loop, Parallel Blocks, Force-Release, Construct, Event. | | |
| **Unit-4** | **Modeling Concepts -III** | **8 hours** |
| **Switch Level Modeling:** Basic Transistor Switches, CMOS Switches, Bi Directional Gates, Time Delays with Switch Primitives, Instantiation with 'Strengths' and 'Delays' Strength Contention with Trireg Nets.<br>**System Tasks, Functions and Compiler Directives:** Parameters, Path Delays, Module Parameters. System Tasks and Functions, File Based Tasks and Functions, Computer Directives, Hierarchical Access, User Defined Primitives | | |
| **Unit-5** | **Sequential Circuits and Test-benches** | **8 hours** |
| **Sequential Circuit Description:** Sequential Models - Feedback Model, Capacitive Model, Implicit Model, Basic Memory Components, Functional Register, Static Machine Coding, Sequential Synthesis.<br><br>**Components Test and Verification:** Test Bench - Combinational Circuits Testing, Sequential Circuit Testing, Test Bench Techniques, Design Verification, Assertion Verification. | | |

**Continuous Assessment Pattern**

| Internal Assessment (IA) | Mid Term Test (MTE) | End Term Test (ETE) | Total Marks |
|---|---|---|---|
| 20 | 30 | 50 | 100 |

| Name of The Course | Advanced VLSI Design | | | |
|---|---|---|---|---|
| Course Code | MVLS5021 | | | |
| Prerequisite | Basic knowledge of semiconductors and its devices | | | |
| | L | T | P | C |
| | 3 | 0 | 0 | 3 |

**Course Objectives:**.

This course is designed to impart the knowledge of VLSI designing methodologies. The mathematical approach in dealing with the designing aspects enables the students to understand the subject in a better way.

**Course Outcomes**

| | |
|---|---|
| **CO1** | Understand the Basics of MOS and Bipolar Transistor Amplifiers |
| **CO2** | Illustrate current mirrors and analyse the performance of various amplifiers with active loads |
| **CO3** | Desaign of Various MOS transistor powered operational Amplifiers |
| **CO4** | Understand and design various oscillators and Conveter circuits using CMOS Transistors |
| **CO5** | Understand the concepts of Switched Capacitor Filters |

**Text Book (s)**


1. N. Weste and K. Eshranghian, "Principles of CMOS VLSI Design", Addison Wesley, 1998.
2. Jacob Backer, Harry W. Li and David E. Boyce, " CMOS Circuit Design, Layout and Simulation ", Prentice Hall of India, 1998..
3. L.Glaser and D. Dobberpuhl, "The Design and Analysis of VLSI, Circuits", Addison Wesley 1993.


Reference Book (s)


1. Randel & Geiger, " VLSI Analog and Digital Circuit Design Techniques" McGraw-Hill,1990.
2. William M. Penny, Lillian Lau, " MOS Integrated Circuits- Theory, Fabrication, Design and System Applications of MOS LSI", Van Nostrand Reihold Company..
3. Sung Ms Kang, Yusuf Lablebici, "CMOS Digital Integrated Circuits Analysis & Design", Tata Mc-Graw Hill.


**Course Content:**

| | | |
|---|---|---|
| **Unit-1** | MOSFETs Fundamentals | **9 hours** |
| Introduction To MOS Circuits: MOS Transistors, MOS Transistor Switches, CMOS Logic, Circuit and System Representations, MOS Transistor Theory - Introduction MOS Device Design Equations, The Complementary CMOS Inverter-DC Characteristics, Static Load MOS Inverters, The Differential Inverter, The Transmission Gate, The Tri State Inverter, Bipolar Devices | | |
| **Unit-2** | Circuit Characterization And Performance Estimation | **8 hours** |
| Resistance Estimation Capacitance Estimation, Inductance, Switching Characteristics CMOSGate Transistor Sizing, Power Dissipation, Sizing Routing Conductors, Charge Sharing, Design Margining, and Reliability. | | |
| **Unit-3** | CMOS Circuits | **8 hours** |
| CMOS Circuit And Logic Design: CMOS Logic Gate Design, Basic Physical Design | | |

| | | |
|---|---|---|
| of Simple Gate, CMOS Logic Structures, Clocking Strategies, I/O Structures, Low Power Design. Basic operation of CMOS inverter, detailed analysis of its noise margin propagation delay, power dissipation concept of layout & area, layout optimization & area estimation for a single as well as combinational logic circuits. | | |
| **Unit-4** | Systems Design And Design Method | **8 hours** |
| Design Strategies CMOS Chip Design Options, Design Methods, Design Capture Tools, Design Verification Tools, Design Economics, Data Sheets, CMOS Testing - Manufacturing Test Principles, Design Strategies for Test, Chip Level Test Techniques, System Level Test Techniques, Layout Design for Improved Testability. | | |
| **Unit-5** | CMOS Sub System Design | **8 hours** |
| Data Path Operations-Addition/Subtraction, Parity Generators, Comparators, Zero/One Detectors, Binary Counters, ALUs, Multiplication, Shifters, Memory Elements, Control-FSM, Control Logic Implementation. | | |

**Continuous Assessment Pattern**

| **Internal Assessment (IA)** | **Mid Term Test (MTE)** | **End Term Test (ETE)** | **Total Marks** |
|---|---|---|---|
| 20 | 30 | 50 | 100 |

| Name of The Course | Analog Filter Design | | | |
|---|---|---|---|---|
| **Course Code** | MVLS5004 | | | |
| **Prerequisite** | Analog Signal Processing | | | |
| | **L** | **T** | **P** | **C** |
| | 3 | 0 | 0 | 3 |

**Course Objectives:**. Analog circuits are essential in interfacing and building amplifiers and low pass filters. This course introduces design methods for CMOS an alog filter circuit.

**Course Outcomes**

| | |
|---|---|
| **CO1** | Acquire a basic knowledge of filters and their characteristics. |
| **CO2** | Develop the ability to analyze and design analog filter circuits**.** |
| **CO3** | Learn noise modeling of CMOS analog circuits |
| **CO4** | Analysis of Butterworth and Chebyshev filters. |
| **CO5** | Design analog filter using recent active building block(CFOA, OTRA, CDTA, etc.) |

**Text Book (s)**

1. Sedra and K. C. Smith, "Microelectronic Circuits", Oxford.
2. G. Daryanani, "Principles of Active Network Synthesis & Design", John Wiley & Sons

**Reference Book (s)**

1. Design of Analog Filters, Van Valkenburg, Oxford.

**Course Content:**

| **Unit-1** | **Basic Concepts** | **8 hours** |
|---|---|---|
| Filters: Types, Specifications and Transfer functions; Circuit elements and scaling; OP-AMP: integrator model & basic circuits; Bode plots. | | |
| **Unit-2** | **Design and analysis of First & Second order Filters** | **8 hours** |
| First order: Bilinear transfer functions, Passive Realization, Active realization, Realization with Bode plots; Second order: Design parameters (ω and Q), Second order circuit. | | |
| **Unit-3** | **Synthesis Techniques** | **8 hours** |
| Biquad Topology: Tow Thomas, KHN, Sallen-Key, Single Amplifier Biquad using Multiple feedback Topology; Inductance Simulation, General impedance converter (GIC) and FDNR. | | |
| **Unit-4** | **Approximation Theory** | **8 hours** |
| Butterworth: Ideal low pass filter, Butterworth response & pole locations, low pass filter specifications; Chebyshev: Chebyshev polynomial, magnitude response, location of Chebyshev poles. | | |
| **Unit-5** | **Study of Filter building blocks & recent trends** | **8 hours** |
| Current mode building blocks and tunable filters using OTA, Current conveyors (CCI, CCII), CFOA, OTRA etc. and recent trends. | | |

**Continuous Assessment Pattern**

| **Internal Assessment (IA)** | **Mid Term Test (MTE)** | **End Term Test (ETE)** | **Total Marks** |
|---|---|---|---|
| 20 | 30 | 50 | 100 |

| Name of The Course | PROFESSIONAL AND COMMUNICATION SKILL | | | |
|---|---|---|---|---|
| Course Code | CENG5001 | | | |
| Prerequisite | -- | | | |
| | L | T | P | C |
| | 0 | 0 | 4 | 2 |

**Course Objectives:**.

To develop the professional and communication skills of learners in a technical environment.
To enable the students to acquire functional and technical writing skills.
To acquire state-of-the-art presentation skills in order to present technical topics to both technical and non-technical audience.

**Course Outcomes**

| | |
|---|---|
| **CO1** | The learners will be able to exhibit their language proficiency and skill in *Describing Technology.* |
| **CO2** | The learners will be able to exhibit their language proficiency and skill in *Investigating and designing using Technology.* |
| **CO3** | Exhibit their language proficiency and skill in Technical Writing and Syntax. |
| **CO4** | Exhibit their language proficiency and skill in Technical Resume and Company Profile Presentation. |
| **CO5** | Exhibit their language proficiency and skill in Pie chart, Bar chart, Line graphs: analysis and interpretation |

**Text Books and Softwares:**

1. English Vocabulary in Use Advanced, McCarthy & Felicity, CUP, 2003
2. Sky Pronunciation CD-ROM
3. Cambridge Advanced Learner's Dictionary CD-ROM
4. English Master : Grammar

**Reference Book (s)**

1. Writing, Researching, Communicating, Keith et al, Tata McGraw-Hill, 1989
2. Advanced English Grammar, Martin, CUP, 2006

**Course Content:**

| **Unit-1** | **Basics of Communication** | **8 hours** |
|---|---|---|
| **Functional Language** | Basic structures- Tense agreement, Prepositional phrases<br>Techno-words : Basic Concepts 62, 63<br>Pronunciation : sounds of syllables: Past tense & plural endings | |
| **Technical Expression** | Organizational techniques in technical writing<br>Guided writing: Paragraph Writing, Note Making | |
| **Presentation Skills** | Techniques of presentation (general topic: speech without visual aids)<br>Listening to speeches and comprehending | |
| **Graphical Skills** | Flow chart: Process and Functional description | |
| **Unit-2** | | **8 hours** |
| **Functional Language** | Basic structures- Voice, Conditionals<br>Techno-words : Basic Concepts 64,65,67<br>Pronunciation : Word Stress: two syllable words | |
| **Technical Expression** | Mechanics of Technical Writing and Syntax<br>Guided writing: Letter and email | |

| | | |
|---|---|---|
| **Presentation Skills** | Interpersonal Communication Skills<br>Writing techniques for Power point presentation, Group Discussion | |
| **Graphical Skills** | Technical Illustrations and Instructions | |
| **Unit-3** | | **8 hours** |
| **Functional Language** | Basic structures- Modal Verbs and Phrasal verbs<br>Techno-words : Basic Concepts 68,69,70,71<br>Pronunciation : Word Stress: compound words | |
| **Technical Expression** | Mechanics of Technical Writing and Syntax<br>Guided writing: Technical Description | |
| **Presentation Skills** | Career advancement: Technical Resume and Company Profile<br>Presentation and Group Discussion | |
| **Graphical Skills** | Pie chart, Bar chart, Line graphs: analysis and interpretation | |
| **Unit-4** | | **8 hours** |
| **Functional Language** | Basic structures- Modal Verbs and Phrasal verbs<br>Techno-words : Basic Concepts 72,73,74, Functional vocabulary 87<br>Pronunciation : Sentence Stress | |
| **Technical Expression** | Guided and Free writing: Abstract and Technical articles | |
| **Presentation Skills** | Nuances of Presentation to a Technical audience | |
| **Graphical Skills** | Oral Presentation of graphical representation | |

**Continuous Assessment Pattern**

| **Internal Assessment (IA)** | **Mid Term Test (MTE)** | **End Term Test (ETE)** | **Total Marks** |
|---|---|---|---|
| 20 | 30 | 50 | 100 |

| Name of The Course | DSP for VLSI | | | |
|---|---|---|---|---|
| Course Code | MVLS5007 | | | |
| Prerequisite | DSP | | | |
| | L | T | P | C |
| | 3 | 0 | 0 | 3 |

**Course Objectives:**

To design and analysis of DSP systems at chip level design

Design the different digital filters with efficient ways using VLSI.

**Course Outcomes**

| | |
|---|---|
| **CO1** | To understand theory of different filters and algorithms |
| **CO2** | understand theory of multirate DSP, solve numerical problems and write algorithms |
| **CO3** | understand theory of prediction and solution of normal equations |
| **CO4** | know applications of DSP at block level. |
| **CO5** | understand theory of adaptive filters and algorithms |

**Text Book (s)**

1. Parhi, K.K., VLSI Digital Signal Processing Systems: Design and Implementation, John Wiley (2007).

2. Oppenheim, A.V. and Schafer, R.W., Discrete-Time Signal Processing, Prentice Hall (2009) 2nd ed

**Reference Book (s)**

1. Mitra, S.K., Digital Signal Processing. A Computer Based Approach, McGraw Hill (2007)3rd ed.

2. Wanhammar, L., DSP Integrated Circuits, Academic Press (1999).*2005, ISBN: 978-0131543188.*

**Course Content:**

| | | |
|---|---|---|
| **Unit-1** | **Introduction to DSP Systems** | **8 hours** |
| Introduction to DSP Systems, Iteration bound, Data Flow graphs (DFGs) representation, Loop Bound, Iteration rate, Critical loop, Critical path, Area-Speed-Power trade-offs, Algorithms for computing iteration bound, Pipelining of FIR Digital Filters, Parallel Processing, Pipelining and Parallel Processing for low power | | |
| **Unit-2** | **Algorithmic Transformations** | **8 hours** |
| Retiming Definitions and properties, Retiming Techniques, Clock period minimization, Unfolding, An algorithm for unfolding, Critical path, Applications of unfolding, Sample period reduction, Folding, Folding order, Folding Factor, register minimization techniques, register minimization in folded architecture, Forward Backward Register Allocation technique, folding of multi-rate systems, Folding Bi-quad filters, Retiming for folding. | | |
| **Unit-3** | **Systolic Architecture Design and Fast Convolution** | **8 hours** |
| Introduction, system array design methodology, FIR systolic arrays, , Systolic Design for space representations containing delays Systolic architecture design methodology, Design examples of systolic architectures, selection of scheduling vector, matrix-matrix multiplication and 2-D systolic array design, Hardware Utilization efficiency, Cook-Toom Algorithm, Wniograd Algorithm, Iterated Convolution, Cyclic Convolution, Design of fast convolution algorithm by inspection. | | |
| **Unit-4** | **Algorithm Strength Reduction in filter** | **8 hours** |
| Introduction, Parallel FIR filters, Polyphase decomposition, Discrete Cosine Transform and Inverse Discrete Cosine Transform, parallel architectures for Rank Order filters. | | |
| **Unit-5** | **Pipelined and Parallel Recursive and Adaptive Filters** | **8 hours** |

| |
|---|
| Introduction, pipelining in 1st order IIR digital filters, pipelining in higher order IIR digital filters, parallel processing for IIR filters, combined pipelining and parallel processing for IIR filters, low power IIR Filter Design using pipelining and parallel processing, pipelined adaptive digital filters. |

**Continuous Assessment Pattern**

| **Internal Assessment (IA)** | **Mid Term Test (MTE)** | **End Term Test (ETE)** | **Total Marks** |
|---|---|---|---|
| 20 | 30 | 50 | 100 |

| Name of The Course | VLSI Testing and Fault Tolerance | | | |
|---|---|---|---|---|
| Course Code | MVLS5008 | | | |
| Prerequisite | | | | |
| | L | T | P | C |
| | 3 | 0 | 0 | 3 |

**Course Objectives:**. This course deals with basics of testing and fault diagnosis in IC design. The combinational and sequential circuits are tested with various test patterns. Self checking circuits and algorithms are also discussed.

**Course Outcomes**

| | |
|---|---|
| **CO1** | Understand various testing techniques. |
| **CO2** | Various physical faults and their modelling |
| **CO3** | Various self test circuits and test algorithms |
| **CO4** | Know fault diagnosis methods for combinational and sequential circuits |
| **CO5** | Verify increasingly complex designs more efficiently and effectively. |

**Course Content:**

| | | |
|---|---|---|
| **Unit-1** | **Physical Fault Modeling And Basics Of Testing** | **8 hours** |
| Physical Faults and their modelling, Stuck at Faults, Bridging Faults, Fault collapsing, Fault Simulation, Deductive, Parallel, and Concurrent Fault Simulation, Introduction to Testing | | |
| **Unit-2** | **Test Generation For Combinational And Sequential Circuits** | **8 hours** |
| Deterministic and Weighted Random Test Pattern Generation, Test generation for combinational logic circuits, Testable combinational logic circuit design, Test generation for sequential circuits, design of testable sequential circuits. | | |
| **Unit-3** | **Design For Testability** | **8 hours** |
| Design for Testability, Ad-hoc design, Generic scan based design, Classical scan based design ,System level DFT approaches, Time Frame Expansion, Controllability and Observability Scan Design, Boundary Scan for Board Level Testing | | |
| **Unit-4** | **Self Test And Test Algorithms** | **8 hours** |
| Built-In Self Test and Totally Self checking circuits, Test pattern generation for BIST , Circular BIST, BIST Architectures, Testable Memory Design -Permanent, Intermittent and Pattern Sensitive Faults, Marching Tests, Test algorithms , Test generation for Embedded RAMs. | | |
| **Unit-5** | **Fault Diagnosis** | **8 hours** |
| Logic Level Diagnosis, Diagnosis by UUT reduction, Fault Diagnosis for Combinational Circuits , Self-checking design, System Level Diagnosis, Concept of Redundancy, Spatial Redundancy, Time Redundancy, Error Correction Codes, Reconfiguration Techniques, Yield Modelling, Reliability and effective area utilization. | | |

**Continuous Assessment Pattern**

| Internal Assessment (IA) | Mid Term Test (MTE) | End Term Test (ETE) | Total Marks |
|---|---|---|---|
| 20 | 30 | 50 | 100 |

| Name of The Course | ASIC Design and FPGA | | | |
|---|---|---|---|---|
| Course Code | MVLS5009 | | | |
| Prerequisite | | | | |
| | L | T | P | C |
| | 3 | 0 | 0 | 3 |

**Course Objectives:**. This course deals with the concepts of ASIC design, ASIC Construction and design using Xilinx

**Course Outcomes**

| | |
|---|---|
| **CO1** | Define the basic concepts of ASIC design and Verilog HDL |
| **CO2** | Express the details of programmable ASICs and FPGAs technologies from ACTEL, ALTERA and XILINX |
| **CO3** | Practice writing the Dataflow and Behavioral models of digital circuits for simulation and synthesis using ASICs and FPGAs |
| **CO4** | Testing and Verification of Register Transfer Level (RTL) models of Digital Circuits using ASICs and FPGAs. |
| **CO5** | Simulate and Synthesize using Xilinx family FPGA |

**Text Book (s):**

1. M.J.S .Smith, - " Application - Specific Integrated Circuits " - Addison -Wesley Longman Inc., 1997
2. R. B. Reese, M A Thornton, "Introduction to Logic Syntehsis Using Verilog HDL," Morgan & Claypool Publishers, 2006

**Reference Book (s)**

1. Skahill, Kevin," VHDL for Programmable Logic", Addison-Wesley, 1996
2. John F. Wakherly, " Digital Design: Principles and Practices", 2nd Edn 1994, Prentice Hall International Edn
3. Charles W. Mckay, "Digital Circuits a proportion for microprocessors", Prentice Hall International Edition.

**Course Content:**

| **Unit-1** | **Introduction To ASIC and HDL** | **8 hours** |
|---|---|---|
| Introduction To ASICS, CMOS Logic And ASIC Library Design,Types of ASICs - Design flow - CMOS transistors CMOS Design rules - Combinational Logic Cell – Sequential logic cell - Data path logic cell - Transistors as Resistors - Transistor Parasitic Capacitance- Logical effort -Library cell design - Library architecture.<br>Review of VHDL/Verilog: Entities and architectures | | |
| **Unit-2** | **Programmable ASICS** | **8 hours** |
| Programmable Asics, Programmable ASIC Logic Cells And Programmable ASIC I/O Cells Anti fuse - static RAM - EPROM and EEPROM technology - PREP benchmarks - Actel ACT - Xilinx LCA - Altera FLEX - Altera MAX DC & AC inputs and outputs -<br>Clock & Power inputs - Xilinx I/O blocks | | |
| **Unit-3** | **Programmable ASIC Interconnect & Software** | **8 hours** |
| Programmable ASIC Interconnect, Programmable ASIC Design Software And Low | | |

| | | |
|---|---|---|
| Level Design Entry Actel ACT -Xilinx LCA - Xilinx EPLD - Altera MAX 5000 and 7000 - Altera MAX 9000<br>- Altera FLEX - Design systems - Logic Synthesis - Half gate ASIC -Schematic entry -<br>Low level design language - PLA tools - EDIF- CFI design representation | | |
| **Unit-4** | **ASIC Construction & FPGA partitioning** | **8 hours** |
| ASIC Construction, Floor Planning, Placement And Routing,System partition - FPGA partitioning - partitioning methods - floor planning - placement - physical design flow - global routing - detailed routing - special routing -circuit extraction - DRC. | | |
| **Unit-5** | **Design using Xilinx** | **8 hours** |
| Design using Xilinx family FPGA | | |

**Continuous Assessment Pattern**

| **Internal Assessment (IA)** | **Mid Term Test (MTE)** | **End Term Test (ETE)** | **Total Marks** |
|---|---|---|---|
| 20 | 30 | 50 | 100 |

| Name of The Course | Embedded Systems Design | | | |
|---|---|---|---|---|
| **Course Code** | MVLS6001 | | | |
| **Prerequisite** | | | | |
| | **L** | **T** | **P** | **C** |
| | 3 | 0 | 0 | 3 |

**Course Objectives:**

This course deals introduction to Embedded Computing, embedded Processors, RTOS Design and Simulation.

**Course Outcomes**

| | |
|---|---|
| **CO1** | understand the basic of Embedded System Design. |
| **CO2** | visualize the role of CISC & amp; RISC in processor operation. |
| **CO3** | differentiate between embedded processor and other general-purpose processors and how to use them in specific application |
| **CO4** | understand RTOS – basics and relevance in embedded system. |
| **CO5** | list Issues involved in embedded system design |

**Text Book (s)**

1. Wayne Wolf, "Computers as Components: Principles of Embedded Computing System Design", Morgan Kaufman Publishers.
2. Jane.W.S. Liu, "Real-Time systems", Pearson Education Asia.
3. Heath, S., Embedded Systems Design, Elsevier Science (2003).

**Reference Book (s)**

1. C. M. Krishna and K. G. Shin, "Real-Time Systems" , McGraw-Hill, 1997
2. Frank Vahid and Tony Givargis, "Embedded System Design: A Unified Hardware/Software Introduction" , John Wiley & Sons.
3. Fisher, J.A., Faraboschi, P. and Young, C., Embedded Computing - A VLIW
4. Approach to Architecture, Compilers and Tools, Morgan Kaufman (2005).

**Course Content:**

| **Unit-1** | **Embedded Processing** | **8 hours** |
|---|---|---|
| Introduction to Embedded Computing, Difference between Embedded and General-Purpose Computing, Characterizing Embedded Computing, Design Philosophies, RISC, CISC, VLIW versus superscalar, VLIW versus DSP Processors, Role of the Compiler, Architectural structures, The data path, Registers and Clusters, Memory Architecture, Branch architecture, Speculation and prediction, Prediction in the embedded domain, Register File Design, Pipeline Design, the control unit, control registers | | |
| **Unit-2** | **Embedded Processors** | **8 hours** |
| Embedded Computers, Characteristics of Embedded Computing Applications, and Challenges in Embedded Computing system design. ARM architecture, Embedded Cores, Soft and Hard Cores, Architecture of Configurable Microblaze soft core, Instruction set, Stacks and Subroutines, Microblaze Assembly Programming, Input-Output interfacing, GPIO, LCD interfacing, Peripherals, DDR Memory, SDRAM, Microblaze interrupts, Timers, Exceptions, Bus Interfacing, DMA, On-chip Peripheral bus (OPB), OPB Arbitration, OPB DMA | | |
| **Unit-3** | **Networks** | **8 hours** |
| Distributed Embedded Architecture- Hardware and Software Architectures, Networks for embedded systems- I2C, CAN Bus, SHARC link supports, Ethernet, Myrinet, Internet, Network-Based design-Communication Analysis, system performance Analysis, Hardware platform design, Allocation and scheduling, Design Example: Elevator Controller. | | |

| Unit-4 | RTOS and Application Design | 8 hours |
|---|---|---|
| Programming embedded systems in assembly and C – Meeting real time constraints –Multi-state systems and function sequences. Embedded software development tools –Emulators and debuggers. Embedded Matlab, Embedded JAVA, Embedded C extensions, Real time operating systems, Embedded RTOS, Real time process scheduling, structure of real time operating system, Memory management in Embedded operating system. File systems in Embedded devices, Different types of locks, Semaphores, Application studies with Vxworks, Montavista Linux etc. | | |
| **Unit-5** | **System Design Techniques and Simulation** | **8 hours** |
| Design Methodologies, Requirement Analysis, Specification, System Analysis and Architecture Design, Quality Assurance. System-on-a-Chip (SoC), IP Blocks and Design Reuse, Processor Cores and SoC, Non-programmable accelerators, reconfigurable logic, multiprocessing on a chip, symmetric multiprocessing, heterogeneous multiprocessing, use of simulators, Compilers, Loaders, Linkers, locators, assemblers, Libraries, post run optimizer, debuggers, profiling techniques, binary utilities, linker script**,** system simulation. | | |

**Continuous Assessment Pattern**

| Internal Assessment (IA) | Mid Term Test (MTE) | End Term Test (ETE) | Total Marks |
|---|---|---|---|
| 20 | 30 | 50 | 100 |

| | | | | | |
|---|---|---|---|---|---|
| **Name of The Course** | Advanced VLSI Technology | | | | |
| **Course Code** | MVLS5003 | | | | |
| **Prerequisite** | | | | | |
| | | **L** | **T** | **P** | **C** |
| | | 3 | 0 | 0 | 3 |

**Course Objectives:**.

A course in VLSI semiconductor devices, to give knowledge about modern CMOS technology, crystal growth, fabrication, and basic properties of silicon wafers. It will focus on lithography, thermal oxidation, (Si/Si)2, interface, dopant diffusion, ion implantation, thin film deposition, etching, and back-end technology

**Course Outcomes**

| | |
|---|---|
| **CO1** | Understand various IC fabrication techniques. |
| **CO2** | Have knowledge of fabrication of various semiconductor components. |
| **CO3** | Understand fundamentals of different deposition techniques for thin film deposition. |
| **CO4** | Learn basics of lithography and application of different lithographic technologies in IC fabrication processes. |
| **CO5** | Understand etching and metallization process and its significance in IC fabrication process. |

**Text Book (s)**

1. W. Wolf, "Modern VLSI design", 4th Edition, PHI Learning, 2009, ISBN 9788120338241.
2. S.M.Sze, "VLSI technology", 2nd Edition, Tata Mc Graw Hill Education, 2003, ISBN 9780070582910

**Reference Book (s)**

1. Douglas Pucknell, "Basic VLSI design", 3rd Edition, PHI Learning, 2011, ISBN 9788120309869

**Course Content:**

| | | |
|---|---|---|
| **Unit-1** | **IC Fabrication Technologies** | **8 hours** |
| Process steps in IC fabrication Crystal growth and wafer preparation- Czochralski process- apparatus- silicon shaping, slicing and polishing- Diffusion of impurities- physical mechanism- Fick's I and II law of diffusion- Diffusion profiles- complementary (erfc) error function- Gaussian profile- Ion implantation- Annealing process- Oxidation process- Lithography- Photolithography, Fine line lithography, electron beam and x-ray lithography- Chemical vapour deposition- epitaxial growth- reactors- metallisation- patterning- wire bonding and packaging – Comparison. | | |
| **Unit-2** | **Fabrication of Semiconductor Devices** | **8 hours** |
| Monolithic components Isolation of components- junction isolation and dielectric isolation- Transistor fabrication- buried layer- impurity profile- parasitic effects- monolithic diodes- schottky diodes and transistors- FET structures- JFET- MOSFET- PMOS and NMOS, control of threshold voltage (Vth)- silicon gate technology- Monolithic resistors- sheet resistance and resistor design- resistors in diffused regions- MOS resistors- monolithic capacitors- junction and MOS structures- IC crossovers and vias | | |
| **Unit-3** | **CMOS Technology** | **8 hours** |
| CMOS technology Metal gate and silicon gate- oxide isolation- Twin well process- Latch up- BiCMOS technology- fabrication steps- circuit design process- stick diagrams- design rules- Capacitance of layers- Delay- Driving large capacitance loads- Wiring capacitance- Basic circuit concepts- scaling of MOS structures- scaling factors- effects of miniaturization. | | |
| **Unit-4** | **CMOS Logic Systems** | **8 hours** |

| | | |
|---|---|---|
| Subsystem design and layout- Simple logic circuits- inverter, NAND gates, BiCMOS circuit, NOR gates, CMOS logic systems – bus lines- arrangements- power dissipation- power supply rail distribution- subsystem design process- design of a 4 bit and 8 bit shifter. | | |
| **Unit-5** | **GaAs Fabrication** | **8 hours** |
| Gallium Arsenide Technology Sub-micro CMOS technology- Crystal structure- Doping process- Channeling effect- MESFET- GaAs fabrication- Device modeling. | | |

**Continuous Assessment Pattern**

| **Internal Assessment (IA)** | **Mid Term Test (MTE)** | **End Term Test (ETE)** | **Total Marks** |
|---|---|---|---|
| 20 | 30 | 50 | 100 |

| Name of The Course | MOS Device Modelling | | | |
|---|---|---|---|---|
| **Course Code** | MVLS5005 | | | |
| **Prerequisite** | | | | |
| | **L** | **T** | **P** | **C** |
| | 3 | 0 | 0 | 3 |

**Course Objectives:**.

This course deals with fundamentals of semiconductor devices, which are undergraduate level, will be reviewed and distributed-constant circuit models will be also provided. Then, in-depth modeling of MOS transistors will be introduced using the textbook. This helps you design VLSIs using the deep sub-micron CMOS in the near future

**Course Outcomes**

| | |
|---|---|
| **CO1** | Explain basic concept of semiconductor devices |
| **CO2** | Design CMOS VLSI chips |
| **CO3** | model, analyze and design different types of MOS devices |
| **CO4** | Learn Parameter Measurement |
| **CO5** | Forecast the future direction of VLSI technologies |

**Text Book (s)**

1. Tsividis, Y., "Operation and Modeling of the MOS Transistor", 2nd ed.,Oxford University Press, 2008.
2. Sze, S.M., "Physics of Semiconductor Devices", John Wiley, 2008.

**Reference Book (s)**

1. Muller, R.S., Kamins, "T.I., and Chan, M., Device Electronics for Integrated Circuits", 3rd ed., John Wiley, 2007.
2. Taur, Y. and Ning, T.H., "Fundamentals of Modern VLSI Devices", Cambridge University Press, 2009.

**Course Content:**

| **Unit-1** | **Semiconductor and Quantum Mechanics Fundamentals** | **8 hours** |
|---|---|---|
| Poisson and Continuity Equations, Recombination, Equilibrium carrier concentrations electron statistics, density of states, effective mass, bandgap narrowing), Review of PN and MS diodes. Basic Quantum Mechanics, Crystal symmetry and band structure, 2D/1D density of states, Tunneling | | |
| **Unit-2** | **Modeling and Simulation of Carrier Transport and MOS Capacitors** | **8 hours** |
| Carrier Scattering (impurity, phonon, carriercarrier, remote/interface), Boltzmann Transport Equation, Drift-diffusion. Modes of operation (accumulation, depletion, strong/weak inversion), Capacitance versus voltage, Gated diode, Non-ideal effects (poly depletion, surface charges), High field effects (tunneling, breakdown). | | |
| **Unit-3** | **MOSFET Modeling** | **8 hours** |
| Introduction Interior Layer, MOS Transistor Current, Threshold Voltage, Temperature Short Channel and Narrow Width Effect, Models for Enhancement, Depletion Type MOSFET, CMOS Models in SPICE, Long Channel MOSFET Devices, Short Channel MOSFET Devices. | | |
| **Unit-4** | **Parameter Measurement** | **8 hours** |
| General Methods, Specific Bipolar Measurement, Depletion Capacitance, Series Resistances, Early Effect, Gummel Plots, MOSFET: Long and Short Channel Parameters, Statistical Modeling of Bipolar and MOS Transistors. | | |
| **Unit-5** | **Advanced Device Technology** | **8 hours** |

| |
|---|
| SOI, SiGe, strained Si, Alternative oxide/gate materials, Alternative geometries (raised source/drain, dual gate, vertical, FinFET), Memory Devices (DRAM, Flash). Sub-micron and Deep sub-micron Device Modeling. |

**Continuous Assessment Pattern**

| **Internal Assessment (IA)** | **Mid Term Test (MTE)** | **End Term Test (ETE)** | **Total Marks** |
|---|---|---|---|
| 20 | 30 | 50 | 100 |

| Name of The Course | Advanced Digital VLSI Design | | | | |
|---|---|---|---|---|---|
| Course Code | MVLS5010 | | | | |
| Prerequisite | | | | | |
| | | L | T | P | C |
| | | | | | |

**Course Objectives:**.

This course deals with the concepts of MOS transistor, Modelling of MOS transistor, CMOS, Latches and Registers.

**Course Outcomes**

| | |
|---|---|
| **CO1** | understand the concepts of MOS devices |
| **CO2** | model MOS transistor |
| **CO3** | **Design latches and registers** |
| **CO4** | **Design data paths** |
| **CO5** | **Understand memory control elements** |

**Text Book (s):**

1. Jan.M.Rabaey., Anitha Chandrakasan Borivoje Nikolic, "Digital Integrated Circuits", Second Edition
2. Neil H.E Weste and Kamran Eshraghian, "Principles of CMOS VLSI Design", 2nd Edition, Addition Wesley, 1998

**Reference Book (s):**

1. Sung-Mo Kang, Yusuf Leblebici, "CMOS Digital IC- Analysis and Design", 3rd Edition, Tata McGraw Hill publication

**Course Content:**

| **Unit-1** | **MOS Transistor** | **8 hours** |
|---|---|---|
| MOS Transistor-Introduction to MOS device, MOS Transistor under static conditions-threshold voltage-Resistive operation-saturation region -channel length modulation-velocity saturation-Hot carrier effect-drain current Vs voltage charts - sub threshold conduction - equivalent resistance-MOS structure capacitance-Design A logic sates using NMOS and PMOS and CMOS devices-Stick Diagram. | | |
| **Unit-2** | **Modelling of MOS Transistor** | **8 hours** |
| Modeling of MOS Transistor using PSPICE-Introduction - Basic Concepts-LEVEL1-LEVEL2-LEVEL3 modeling technique-various model comparison. Static CMOS inverter-Evaluating the Robustness of CMOS Inverter. Performance of CMOS inverter: Dynamic Behavior-computing the capacitance-propagation delay sizing inverter for performance-sizing a chain of invertors - Dynamic power consumption-static consumption | | |
| **Unit-3** | **CMOS** | **8 hours** |
| Static CMOS design-complementary CMOS - static properties- complementary CMOS design-Power consumption in CMOS logic gates-dynamic or glitching transitions - Design techniques to reduce switching activity - Radioed logic-DC VSL - pass transistor logic - Differential pass transistor logic -Sizing of level restorer-Sizing in pass transistor-Dynamic CMOS design-Basic principles - Domino logic-optimization of Domino logic-NPCMOS-logic style selection -Designing logic for reduced supply voltages | | |
| **Unit-4** | **Latches & Registers** | **8 hours** |

| | | |
|---|---|---|
| Timing metrics for sequential circuit -latches Vs registers -static latches and registers - Bistability principle - multiplexer based latches-master slave edge triggered registers- non-ideal clock signals-low voltage static latches-static SR flip flop - Dynamic latches and registers-C2MOS register - Dual edge registers-True single phase clocked registers-pipelining to optimize sequential circuit latch Vs register based pipelines-non-Bistable sequential circuit-Schmitt trigger-mono stable - Astable -sequential circuit - choosing a clocking strategy. | | |
| **Unit-5** | **Data Path Operations** | **8 hours** |
| Data Path Operations Addition/Subtraction - Comparators- Zero/One Detectors- Binary Counters- ALUs- Multiplication- Shifters- Memory elements- control : Finite-State Machines. | | |

**Continuous Assessment Pattern**

| **Internal Assessment (IA)** | **Mid Term Test (MTE)** | **End Term Test (ETE)** | **Total Marks** |
|---|---|---|---|
| 20 | 30 | 50 | 100 |

| Name of The Course | Low power VLSI Design | | | |
|---|---|---|---|---|
| Course Code | MVLS5011 | | | |
| Prerequisite | | | | |
| | L | T | P | C |
| | 3 | 0 | 0 | 3 |

**Course Objectives:**. This course deals with issues and models to design low-power VLSI circuits, fundamentals of power dissipation in microelectronic devices, will be able to estimate power dissipation due to switching, short circuit.

**Course Outcomes**

| | |
|---|---|
| **CO1** | analyze and design low-power VLSI circuits using different circuit technologies and design levels. |
| **CO2** | design chips used for battery-powered systems |
| **CO3** | design high-performance circuits not exceeding power limits |
| **CO4** | Design and test of low-voltage CMOS circuits. |
| **CO5** | Learn architecture level estimation and synthesis |

**Text Book (s)**

1. Roy, K. and Prasad, Sharat C., "Low Power CMOS VLSI: Circuit Design" , John Wiley, 2009.

2. Chandrakasan, A.P. and Broderson, R.W., "Low Power Digital CMOS Design", Kluwer, 1995.

**Reference Book (s)**

1. Rabaey, J.M. and Pedram, M., " Low Power Design Methodologies", Springer 1996.

2. Yeo, K.S. and Roy K., Low Voltage, "Low Power VLSI Subsystems", McGraw Hill, 2004.

3. Sanchez-Sinencio, E. and Andreou, A.G., " Low-Voltage/Low-Power Integrated

**Course Content:**

| **Unit-1** | **Low Power Microelectronics** | **8 hours** |
|---|---|---|
| Retrospect and Prospect, Fundamentals of power dissipation in microelectronic devices, Estimation of power dissipation due to switching, short circuit, subthreshold leakage, and diode leakage currents. | | |
| **Unit-2** | **Device & Technology Impact on Low Power** | **8 hours** |
| Dynamic dissipation in CMOS, Transistor sizing & gate oxide thickness, Impact of technology Scaling, Technology & Device innovation. | | |
| **Unit-3** | **Simulation Power and Probabilistic power analysis** | **8 hours** |
| SPICE circuit simulators, gate level logic simulation, capacitive power estimation, static state power, gate level capacitance estimation, architecture level analysis, data correlation analysis in DSP systems. Monte Carlo simulation. Random logic signals, probability & frequency, probabilistic power analysis techniques, signal entropy. | | |
| **Unit-4** | **Low Voltage Technologies and Circuits** | **8 hours** |
| Threshold Voltage Scaling and Control, Multiple Threshold CMOS (MTCMOS), Substrate Bias Controlled Variable Threshold CMOS, Testing Issues: Design and test of low-voltage CMOS circuits. | | |
| **Unit-5** | **Algorithm and architectural level methodologies** | **8 hours** |
| Introduction, design flow, algorithmic level analysis and optimization, Architectural level estimation and synthesis. | | |

**Continuous Assessment Pattern**

| Internal Assessment (IA) | Mid Term Test (MTE) | End Term Test (ETE) | Total Marks |
|---|---|---|---|
| 20 | 30 | 50 | 100 |

| Name of The Course | Sensor Technology and MEMS | | | |
|---|---|---|---|---|
| Course Code | MVLS5014 | | | |
| Prerequisite | | | | |
| | L | T | P | C |
| | 3 | 0 | 0 | 3 |

**Course Description:**

This course deals with study of different Sensors and MEMS technology

**Course Outcomes**

| | |
|---|---|
| **CO1** | Understand working of sensors |
| **CO2** | know microsystems and MEMES |
| **CO3** | Know materials used for MEMS |
| **CO4** | Understand fabrication process |
| **CO5** | Know design process of microsystem |

**Text Book (s):**

1. Integrated Sensors, Microp-actuators and micro-systems (MEMS): K.D. (Guest

Editor) , Special Issue of proceedings of IEEE, Vol. 86, No.8, August 1998

2. RF MEMS: Theory, Design, and Technology: Gabriel M. Rebeiz, Wiley, 2003.

**Reference Book (s)**

1. Fundamentals of Microfabrication : Marc Madou, CRC Press, 1997.

**Course Content:**

| **Unit-1** | **Overview of Sensors** | **8 hours** |
|---|---|---|
| Classification of physical sensors, Integrated, Intelligent, or Smart sensors, Sensor Principles and Examples : Thermal sensors, Electrical Sensors, Mechanical Sensors, Chemical and Biosensors, Case study on strain sensors, Temperature sensors, Pressure sensors, Humidity sensors, Accelerometers, Gyroscopes , RF MEMS Switch, phase shifter, and smart sensors. | | |
| **Unit-2** | **Microsystems** | **8 hours** |
| MEMS and Microsystems, Microsystems and microelectronics, Microsystems and miniaturization, Working principle of micro system, Micro sensors, Micro actuators, MEMS with Micro actuators | | |
| **Unit-3** | **Materials For MEMS** | **8 hours** |
| Substrate and wafer, silicon as a substrate material, silicon compound, silicon Piezo-resistors, Gallium Arsenide, quartz, Piezoelectric crystals, polymers and packaging Materials. | | |
| **Unit-4** | **Fabrication Process** | **8 hours** |
| Photolithography, Ion implantation, Oxidation, Chemical vapor deposition (CVD), Physical vapor deposition, Deposition by Epitaxy, Etching.Manufacturing Process - Bulk Micromachining, Surface Micromachining, LIGA Process | | |
| **Unit-5** | **Micro system Design** | **8 hours** |
| Design consideration, process design, Mechanical design, Mechanical design using MEMS. Mechanical packaging of Microsystems, Microsystems packaging, interfacing in Microsystems packaging, packaging technology, selection of packaging materials, signal mapping and transduction. MEMS for RF Applications: Need for RF MEMS components in communications, space and defense applications | | |

**Continuous Assessment Pattern**

| Internal Assessment (IA) | Mid Term Test (MTE) | End Term Test (ETE) | Total Marks |
|---|---|---|---|
| 20 | 30 | 50 | 100 |

| Name of The Course | Nano-Electronics | | | |
|---|---|---|---|---|
| Course Code | MVLS5015 | | | |
| Prerequisite | | | | |
| | L | T | P | C |
| | 3 | 0 | 0 | 3 |

**Course Objectives:**.

1.Understand the fundamental forces controlling the dynamic and static response of materials at the Nano- scale.
2. To have comprehensive understanding of state-of-the-art Nano-fabrication methods.
3. To have knowledge of processing conditions to functional nanomaterials.
4. To scalable system for the continuous production of nanomaterials.
5. To understand the state-of-the-art characterization methods for nanomaterials.

**Course Outcomes**

| | |
|---|---|
| **CO1** | Understand the fundamental forces controlling the dynamic and static response of materials at the Nano-scale.. |
| **CO2** | To demonstrate a comprehensive understanding of state-of-the-art Nano-fabrication method |
| **CO3** | To determine and evaluate processing conditions to functional nanomaterials. |
| **CO4** | Design and analyse scalable system for the continuous production of nanomaterials. |
| **CO5** | Understand the state-of-the-art characterization methods for nanomaterials. |

**Text Book (s):**

1. Nanoelectronics & Nanosystems: From Transistor to Molecular & Quantum Devices: Karl Goser, Jan Dienstuhl.

**Reference Book (s)**

1. Rainer Waser (Ed.), Nanoelectronics and Information Technology: Advanced Electronic Materials and Novel Devices, Wiley-VCH, 2003
2. Microfabrication by Marc Madaon, CRC Press

**Course Content:**

| **Unit-1** | **Introduction to nanoelectronics** | |
|---|---|---|
| Recent past, the present and its challenges, Future, Overview of basic Nanoelectronics, Physics of solid state, Structure - Energy band - Quantum mechanics. | | |
| **Unit-2** | **Fundamentals of Nanoelectronics** | **8 hours** |
| Fundamentals of logic devices:- Requirements, dynamic properties, threshold gates, physical limits to computations, concepts of logic devices:- classifications , two terminal devices, field effect devices, coulomb blockade devices, spintronics , quantum cellular automata – quantum computing ; performance of information processing systems;- basic binary operations, measure of performance processing capability of biological neurons, performance estimation for the human brain. Ultimate computation:- power dissipation limit – dissipation in reversible computation – the ultimate computer. | | |
| **Unit-3** | **Molecular Electronics Components** | **8 hours** |
| Characterization of switches and complex molecular devices, polyphenylene based Molecular rectifying diode switches. Technologies, Single Electron Devices, Quantum Mechanical Tunnel Devices, Quantum Dots & Quantum wires. | | |
| **Unit-4** | **Nanocomputers** | **8 hours** |

| | | |
|---|---|---|
| Nanoelectronic & Nanocomputer architectures and nanotechnology: Introduction to nanoelectronic and nanocomputers, Quantum DOT cellular Automata (QCA), Single electron circuits, molecular circuits Nanocomputer Architecture. | | |
| **Unit-5** | **Silicon MOSFETs & Quantum Transport Devices** | **8 hours** |
| Silicon MOSFETS - Novel materials and alternate concepts:- fundamentals of MOSFET Devices, scaling rules, silicon-dioxide based gate dielectrics, metal gates, junctions & contacts, advanced MOSFET concepts, Quantum transport devices based on resonant tunneling:- Electron tunneling, resonant tunneling diodes – resonant tunneling devices; Single electron devices for logic applications:- Single electron devices – applications of single electron devices to logic circuits. | | |

**Continuous Assessment Pattern**

| **Internal Assessment (IA)** | **Mid Term Test (MTE)** | **End Term Test (ETE)** | **Total Marks** |
|---|---|---|---|
| 20 | 30 | 50 | 100 |

| Name of The Course | Design of Semiconductor Memories | | | |
|---|---|---|---|---|
| Course Code | MVLS5016 | | | |
| Prerequisite | | | | |
| | L | T | P | C |
| | 3 | 0 | 0 | 3 |

**Course Objectives:**.

1. Comprehend the concept of memory structures, reliability and radiation effects.
2. Have a knowledge on Memory fault modelling, Testing and design for fault tolerance.

**Course Outcomes**

| | |
|---|---|
| **CO1** | Select architecture and design semiconductor memory circuits and subsystems. |
| **CO2** | Know non-volatile memory architecture |
| **CO3** | Identify various fault models, modes and mechanisms in semiconductor memories and their testing procedures. |
| **CO4** | Understand reliability issues and RAM failures |
| **CO5** | Know about packaging technologies of memory |

**Text Book (s)**

1. Ashok K. Sharma, "Semiconductor Memories Technology, Testing and Reliability", Prentice-Hall of india Private Limited, New Delhi, 1997.
2. Tegze P. Haraszti," CMOS Memory Circuits", Kluwer Academic Publishers, 2001

**Reference Book (s)**

1. Betty Prince, "Emerging Memories: Technologies and Trends", Kluwer academic publishers, 2002
2. Kiyoo Itoh, "VLSI memory chip design", Springer International Edition

**Course Content:**

| **Unit-1** | **RAM Technologies** | **8 Hours** |
|---|---|---|
| Static Random Access Memories: SRAM Cell Structures-MOS SRAM Architecture-MOS SRAM Cell and Peripheral Circuit Operation-Bipolar SRAM Technologies- SOI Technology-Advanced SRAM Architectures and Technologies-Application Specific SRAM- Dynamic Random Access Memories: DRAM Technology Development-CMOS DRAMs-DRAMs Cell Theory and Advanced Cell Structures -BiCMOS, DRAMs-Soft Error Failures in DRAMs-Advanced DRAM Designs and Architecture-Application, Specific DRAMs. | | |
| **Unit-2** | **Nonvolatile Memories** | **8 hours** |
| Masked Read-Only Memories (ROMs)-High Density ROMs-PROMs-Bipolar PROMs-CMOS, PROMs-Erasable (UV) - EPROM-Floating-GateEPROM Cell-One-Time Programmable (OTP) EPROMs-EEPROM-EEPROM Technology And Arcitecture-Nonvolatile SRAM-Flash Memories (EPROMs or EEPROM)-Advanced Flash Memory Architecture | | |
| **Unit-3** | **Memory Fault Modelling, Testing and design for Fault Tolerance** | **8 hours** |
| RAM Fault Modeling, Electrical Testing, Pseudo Random Testing-Megabit DRAM Testing-Nonvolatile Memory Modeling and Testing-IDDQ Fault Modeling and Testing- Application Specific Memory Testing | | |
| **Unit-4** | **Reliability and Radiation Effects** | **8 hours** |
| General Reliability Issues-RAM Failure Modes and Mechanism-Nonvolatile Memory Reliability-Reliability Modeling and Failure Rate Prediction-Design for Reliability-Reliability Test Structures-Reliability Screening and Qualification. RAM Fault Modeling, | | |

| | | |
|---|---|---|
| Electrical Testing, Psuedo Random Testing-Megabit DRAM Testing-Nonvolatile Memory Modeling and Testing-IDDQ Fault Modeling and Testing-Application Specific Memory Testing. | | |
| **Unit-5** | **Packaging Technologies** | **8 hours** |
| Radiation Effects-Single Event Phenomenon (SEP)-Radiation Hardening Techniques-Radiation Hardening Process and Design Issues-Radiation Hardened Memory Characteristics-Radiation Hardness Assurance and Testing - Radiation Dosimetry-Water Level Radiation Testing and Test Structures. Ferroelectric Random Access Memories (FRAMs)-Gallium Arsenide (GaAs) FRAMs-Analog Memories-Magnetoresistive. Random Access Memories (MRAMs) -Experimental Memory Devices. Memory Hybrids and MCMs (2D)-Memory Stacks and MCMs (3D)-Memory MCM Testing and Reliability Issues-Memory Cards-High Density Memory Packaging Future Directions. | | |

**Continuous Assessment Pattern**

| **Internal Assessment (IA)** | **Mid Term Test (MTE)** | **End Term Test (ETE)** | **Total Marks** |
|---|---|---|---|
| 20 | 30 | 50 | 100 |

| Name of The Course | Advanced Analog VLSI Design | | | |
|---|---|---|---|---|
| Course Code | MVLS5017 | | | |
| Prerequisite | | | | |
| | L | T | P | C |
| | 3 | 0 | 0 | 3 |

**Course Objectives:**

1. Recognize transistor amplifiers.
2. Design multistage MOS amplifiers.

.

**Course Outcomes**

| | |
|---|---|
| **CO1** | demonstrate the use of analog circuit analysis techniques to analyze the operation and behavior of various analog integrated circuits. |
| **CO2** | demonstrate their knowledge by designing analog circuits. |
| **CO3** | compute the gain, power, and bandwidth of analog circuits. |
| **CO4** | Understand the concept of different parameters like gain, power, and bandwidth. |
| **CO5** | understand the Switched capacitor circuits and data converters. |

**Text Book (s)**

1. Paul B Gray and Robert G Meyer, "Analysis and Design of Analog Integrated Circuits".

2. D. A. Johns and Martin, Analog Integrated Circuit Design, John Wiley, 1997.

**Reference Book (s)**

1. R Gregorian and G C Temes, Analog MOS Integrated Circuits for Signal Processing, John Wiley, 1986.

2.R L Geiger, P E Allen and N R Strader, VLSI Design Techniques for Analog & Digital Circuits, McGraw Hill, 1990.

**Course Content:**

| **Unit-1** | **MOS & BJT Transistor Amplifiers** | **8 hours** |
|---|---|---|
| Single transistor Amplifiers stages: Common Emitter, Common base, Common Collector, Common Drain, Common Gate & Common Source Amplifiers<br>Multiple Transistor Amplifier stages: CC-CE, CC-CC, & Darlington configuration, Cascode configuration, Active Cascode. Differential Amplifiers: Differential pair & DC transfer characteristics. | | |
| **Unit-2** | **Current Mirrors, Active Loads & References** | **8 hours** |
| Current Mirrors: Simple current mirror, Cascode current mirrors Widlar current mirror, Wilson Current mirror, etc. Active loads, Voltage & current references. Analysis of Differential Amplifier with active load, supply and temperature independent biasing techniques, Frequency Response, | | |
| **Unit-3** | **Operational Amplifier** | **8 hours** |
| Applications of operational Amplifier, theory and Design; Definition of Performance Characteristics; Design of two stage MOS Operational Amplifier, two stage MOS operational Amplifier with cascodes, MOS telescopic-cascode operational amplifiers,MOS Folded-cascode operational amplifiers, Bipolar operational amplifiers. Frequency response & compensation.. | | |
| **Unit-4** | **Nonlinear Analog Circuits** | **8 hours** |
| Analysis of four quadrant and variable Tran conductance multiplier, Voltage controlled oscillator, Comparators, Analog Buffers, Source Follower and Other Structures. Phase Locked Techniques; | | |

| | | |
|---|---|---|
| Phase Locked Loops (PLL), closed loop analysis of PLL. Digital-to-Analog (D/A) and Analog-to-Digital (A/D) Converters | | |
| **Unit-5** | **OTA & Switched Capacitor filters** | **8 hours** |
| OTA Amplifiers. Switched Capacitor Circuits and Switched Capacitor Filters. | | |

**Continuous Assessment Pattern**

| **Internal Assessment (IA)** | **Mid Term Test (MTE)** | **End Term Test (ETE)** | **Total Marks** |
|---|---|---|---|
| 20 | 30 | 50 | 100 |

| Name of The Course | Physical Design Automation | | | |
|---|---|---|---|---|
| Course Code | MVLS6002 | | | |
| Prerequisite | | | | |
| | L | T | P | C |
| | 3 | 0 | 0 | 3 |

**Course Objectives:**.

1. Learn automation process used in VLSI system design
2. Understand various physical design CAD tools and designing algorithm.

**Course Outcomes**

| | |
|---|---|
| **CO1** | know automation process for VLSI System design. |
| **CO2** | Understanding of fundamentals for various physical design CAD tools. |
| **CO3** | Know floor-planning and PIN assignment |
| **CO4** | Learn to implement different routing algorithms |
| **CO5** | Develop and enhance the existing algorithms and computational techniques for physical automation |

**Text Book (s)**

1. Sung Kyu Lim, Practical Problems for VLSI Physical Design Automation, Springer Publications
2. Majid Sarrafzadeh and C. K. Wong, An Introduction to VLSI Physical Design, McGraw Hill, 1996

**Reference Book (s)**

1.Computer Aided Logical Design with Emphasis on VLSI – Hill & Peterson, Wiley,1993.

2. Naveed Sherwani, Algorithms for VLSI Physical Design Automation, Springer Publications.
3. Modern VLSI Design: Systems on silicon – Wayne Wolf, Pearson Education Asia, 2nd

| **Unit-1** | **Data Structures and Basic Algorithms** | **8 hours** |
|---|---|---|
| Basic Terminology, Complexity Issues and NP-hardness, Basic Algorithms, Basic Data Structures, Graph Algorithms for Physical design. | | |
| **Unit-2** | Partitioning | **8 hours** |
| Problem Formulation, Classification of Partitioning Algorithms, Group Migration Algorithms, Simulated Annealing and Evolution, Other Partitioning Algorithms. Performance Driven Partitioning | | |
| **Unit-3** | **Floorplanning and Pin Assignment** | **8 hours** |
| Floorplanning, Chip planning, Pin Assignment. Global Routing: Problem Formulation, Classification of Global Routing, Maze Routing Algorithms, Line-Probe Algorithms, Shortest Path Based Algorithms, Steiner Tree based Algorithms Integer Programming Based Approach, Performance Driven Routing. | | |
| **Unit-4** | **Detailed Routing** | **8 hours** |
| Problem Formulation, Classification of Routing Algorithms, Single-Layer Routing Algorithms, Two-Layer Channel Routing Algorithms, Three-Layer Channel Routing Algorithms, Multi-Layer Channel Routing Algorithms, Switchbox Routing Algorithms | | |
| **Unit-5** | **Over-the-Cell Routing and Via Minimization** | **8 hours** |
| Over-the-cell Routing, Via Minimization. Clock and Power Routing: Clock Routing, Power and Ground Routing. Compaction: Problem Formulation, Classification of Compaction Algorithms, One-Dimensional Compaction, Two-Dimensional Compaction | | |

**Continuous Assessment Pattern**

| Internal Assessment (IA) | Mid Term Test (MTE) | End Term Test (ETE) | Total Marks |
|---|---|---|---|
| 20 | 30 | 50 | 100 |

| Name of The Course | System-on-Chip Design | | | |
|---|---|---|---|---|
| Course Code | MVLS6003 | | | |
| Prerequisite | | | | |
| | L | T | P | C |
| | 3 | 0 | 0 | 3 |

**Course Objectives:**.

1. Apply concepts of semiconductor devices to design and analyze circuits.
2. To prepare students to know the characteristics of different semiconductor devices.
3. Apply fundamentals of semiconductor devices in electronics projects in circuit design, evaluation and analysis.
4. Explain the fundamental principles necessary for the analysis and design of analog integrated circuits at transistor level.

**Course Outcomes**

| | | |
|---|---|---|
| **CO1** | Define the hardware and software structures used to implement and model inter-component communication in System on Chip. | |
| **CO2** | Describe the details of subsystem components like Adders, Multipliers and ALUs etc. | |
| **CO3** | Practice writing the Behavioral models of digital circuits for simulation and synthesis using SystemC, including transactional modelling. | |
| **CO4** | Learn Testing and Verification of system level designs using SystemC. | |
| **CO5** | Simulate and Synthesize using SystemC. | |

**Text Book (s)**


1. Wolf, W., "Modern VLSI Design: System-on-chip Design", 3rd ed., Prentice Hall 2002.
2. Lin, S. Y.L., "Essential Issues in SOC Design: Designing Complex Systems-On-Chip", Springer ,2006.
3. D. Black, J. Donovan, B. Bunton, A. Keist, "SystemC: From the Ground Up", Second Edition, Springer, 2010.


**Reference Book (s)**


1. Asheden, P.J. and Mermet J., "System-on-Chip Methodologies and Design Languages", Kluwer Academic, 2002.
2. Erbas, C., "System-Level Modelling and Design Space Exploration for Multiprocessor Embedded System-on-Chip Architectures", Amsterdam University Press, 2007.


**Course Content:**

| Unit-1 | Introduction to SOC Design/Overview | 8 hours |
|---|---|---|
| Introduction, Integrated Circuit Manufacturing, CMOS Technology, Integrated Circuit Design Techniques, Fabrication Processes, Transistors, Wires and Vias, Design Rules Layout Design and Tools | | |
| **Unit-2** | **SoC Architecture Design** | **8 hours** |
| Introduction, Front-end chip design, Back-end chip design, Integration platforms and SoC Design, Function Architecture Co-design, Designing Communication Networks, System Level Power Estimation and Modeling, Transaction Level Modeling, Design Space Exploration, Software design in SoCs. | | |
| **Unit-3** | **Basic SoC Subsystem Design** | **8 hours** |

| | | |
|---|---|---|
| Introduction. Subsystem Design Principles. Combinational Shifters. Adders. ALUs. Multipliers. High-Density Memory. Field-Programmable Gate Arrays. Programmable Logic Arrays. | | |
| **Unit-4** | **High level HDL for SoC Design- SystemC** | **8 hours** |
| Introduction of SystemC, Transaction-Level Modeling (TLM) and Electronic System-Level (ESL) languages, SystemC Class Concepts for Hardware, Overview of SystemC Components. | | |
| **Unit-5** | **SoC Design and Test Optimization** | **8 hours** |
| Design methodologies for SoC, Noise and signal integrity analysis, System Integration issues for SoC, SoC Test Scheduling and Test Integration, SoC Test Resource partition. | | |

**Continuous Assessment Pattern**

| **Internal Assessment (IA)** | **Mid Term Test (MTE)** | **End Term Test (ETE)** | **Total Marks** |
|---|---|---|---|
| 20 | 30 | 50 | 100 |

| Name of The Course | Reconfigurable Computing | | | |
|---|---|---|---|---|
| Course Code | MVLS5018 | | | |
| Prerequisite | | | | |
| | L | T | P | C |
| | 3 | 0 | 0 | 3 |

**Course Objectives:**.

Understand concept of Reconfigurable Computing and their applications

**Course Outcomes**

| | |
|---|---|
| **CO1** | Understand parallelism and pipelining concepts, the design aspects and challenges. |
| **CO2** | Evaluate the issues in vector and array processors. |
| **CO3** | Study and analyze the high performance scalable multithreaded and multiprocessor |
| **CO4** | Know Reconfigurable Design |
| **CO5** | know Reconfigurable Devices application |

**Text Book (s)**

1 C. Maxfield, The Design Warrior's Guide to FPGAs, Newnes, 2004, ISBN: 978-0750676045

2 M. Gokhale and P. Graham, Reconfigurable Computing: Accelerating Computation with Field-Programmable Gate Arrays, Springer, 2005, ISBN: 978-0-387-26105-8.

3 C. Bobda, Introduction to Reconfigurable Computing: Architectures, Algorithms and Applications, Springer, 2007, ISBN: 978-1402060885.

**Reference Book (s)**

1. P. Lysaght and W. Rosenstiel (eds.), New Algorithms, Architectures and Applications for Reconfigurable Computing, Springer, 2005, ISBN: 978-1402031274.

2. D. Pellerin and S. Thibault, Practical FPGA Programming in C, Prentice-Hall, 2005, ISBN: 978-0131543188.

3. W. Wolf, FPGA-based System Design, Prentice-Hall, 2004, ISBN: 0-13-142461-0.

4. R. Cofer and B. Harding, Rapid System Prototyping with FPGAs: Accelerating the Design Process, Newnes, 2005, ISBN: 978-0750678667.

**Course Content:**

| Unit-1 | Introduction of RC | 8 hours |
|---|---|---|
| Reconfigurable Computing Basics, Reconfigurable Computing Hardware Components, Custom Computing, Machine Overview, Comparison of Computing Machines, Interconnects, Delays in VLSI Structures, control path and data path, logic minimization. | | |
| **Unit-2** | **FPGA Architectures** | **8 hours** |
| Introduction, Technology-independent optimization, FPGA Mapping, FPGA Partitioning and Placement, Routing, Computing Elements, LUT's, LUT Mapping, ALU and CLB's, Retiming, Multi-FPGA Partitioning, Logic Emulation, Power Reduction Techniques for FPGAs. | | |
| **Unit-3** | **RC Architectures** | **8 hours** |
| Device characteristics, The Systolic Model, Fine-grained architecture, Coarse-grained architecture, Comparison of different architectures, Function-Unit Architectures, Logic Emulation Architectures, Programming Reconfigurable Computers, Logic Cell and Data path Mapping, Hardware/Software Co-design, Systolic Loop Transformations, Software Pipelining, MATRIX and RaPiD, Module Generators. | | |
| **Unit-4** | **Reconfigurable Design** | **8 hours** |

| | | |
|---|---|---|
| Temporal portioning algorithms, Online temporal placement, Device space management, Binding Time and Programming Styles, Overheads, Data Density, Data BW, Function density, Function diversity, Interconnect methods, Contexts, Context switching; Area calculations for PE; Efficiency, ISP, Hot Reconfiguration, Partial reconfigurable design and Dynamic Reconfiguration design. | | |
| **Unit-5** | **RC Applications** | **8 hours** |
| Reconfigurable Coprocessors, Reconfigurable Memory Security, Reconfigurable Weather Radar Data Processing, Dynamically Reconfigurable Adaptive Viterbi Decoder, High Speed Data Acquisition System for Space Applications. | | |

**Continuous Assessment Pattern**

| **Internal Assessment (IA)** | **Mid Term Test (MTE)** | **End Term Test (ETE)** | **Total Marks** |
|---|---|---|---|
| 20 | 30 | 50 | 100 |

| Name of The Course | Packaging and Interconnect Analysis | | | |
|---|---|---|---|---|
| Course Code | MVLS6005 | | | |
| Prerequisite | | | | |
| | L | T | P | C |
| | 3 | 0 | 0 | 3 |

**Course Objectives:**. Analysis and design for high-performance interconnects at both IC and packaging levels, including interconnect modeling, delay modeling for devices and interconnects, timing-driven placement, interconnect topology construction, buffer insertion, device and wire sizing, clock network design, thermal modeling, analysis, and thermal-based placement

**Course Outcomes**

| | |
|---|---|
| **CO1** | understand problems in modeling and design of high-performance VLSI |
| **CO2** | Learn delay calculations |
| **CO3** | Optimize interconnection and topology |
| **CO4** | Know clock design for interconnection |
| **CO5** | Demonstrate thermal modelling and analysis |

**Text Book (s)**

1. M. Celik, L. Pileggi, A. Odabasioglu, IC Interconnect Analysis, Kluwer Academic Publishers, 2002.
2. C. K. Cheng, J. Lillis, S. Lin, N. Chang, Interconnect Analysis and Synthesis, John Wiley & Sons, Inc. 2000.

**Reference Book (s)**

1.J. M. Rabaey, A. Chandrakasan, B. Nikoli´c, Digital Integrated Circuits A Design Perspective, Pearson Education, Inc. 2003

2. N. Menezes, L. Pileggi, Analyzing On-chip Interconnect Effects, Chapter 16 in Design of High-Performance Microprocessor Circuits, IEEE Press, 2001.

3. H. B. Bakoglu, Circuits, Interconnects, and Packaging for VLSI, Addison-Wesley Publishing Company, 1990

**Course Content:**

| Unit-1 | Introduction | 8 hours |
|---|---|---|
| Introduction, Functions of an electronic packages, Brief history of electronic packaging, Packaging Hierarchy, Challenges of Interconnect Design, Modeling of VLSI Interconnects, Laplace transform, Elmore delay model, Moment Computation, Asymptotic waveform evaluation, Pade via Lanczos and transmission line modeling. | | |
| **Unit-2** | **Delay Calculation** | **8 hours** |
| Delay calculating: Devices modeling, R(L)C Delay Calculation. Overview of Layout Design, and Optimization Techniques. Delay Budgeting, Net-based Timing-driven Placement, and Path-base Timing-driven Placement. | | |
| **Unit-3** | **Device , Topology and Interconnect Optimization** | **8 hours** |
| Transistor Ordering, Device Sizing, and Buffer Insertion. Topology Optimization: Wirelength Minimization, Pathlength Minimization, and Delay Minimization.<br>Interconnect Sizing: Local Refinement-based, Dynamic Programming-based, Sensitivity-based, and Mathematical Programming. Simultaneous Device and Interconnect Sizing, Simultaneous Topology Construction, Buffer Insertion, Buffer Sizing, and Interconnect Sizing. | | |
| **Unit-4** | **Clock Design and Noise Modeling** | **8 hours** |

| | | |
|---|---|---|
| Clock Network Design: Zero-Skew, Bounded-Skew, Buffer and Wire Optimization, Non-Tree Routing, and Clock Schedule.<br>Noise Modeling, Avoiding and Control: Simultaneous Switching Noise, Reflection Noise, Coupling Noise, Power/Ground Design, Topology Selection, Optimal Termination, Track Permutation, Layer Assignment, Buffer Insertion, and Interconnect Sizing and Spacing | | |
| **Unit-5** | **Thermal Modeling and Analysis** | **8 hours** |
| Thermal Modeling, Analysis, and Thermal-aware Design: Compact Thermal Modeling, Electro-thermal Simulation, Thermal Characterization of Stacked Dies, and Thermal Based Placement | | |

**Continuous Assessment Pattern**

| **Internal Assessment (IA)** | **Mid Term Test (MTE)** | **End Term Test (ETE)** | **Total Marks** |
|---|---|---|---|
| 20 | 30 | 50 | 100 |

| Name of The Course | EMI and EMC in System Design | | | |
|---|---|---|---|---|
| Course Code | MVLS6006 | | | |
| Prerequisite | | | | |
| | L | T | P | C |
| | 3 | 0 | 0 | 3 |

**Course Objectives:**.

Understand basics of electro-magnetic Interference and describes the concepts of its effects in system designing. The EMI measurements, EMI Control methods and Standards

**Course Outcomes**

| | |
|---|---|
| **CO1** | Understand basic concept of electro-magnetic Interference. |
| **CO2** | **Know methods for EMI measurements** |
| **CO3** | **Learn EMC standards and regulations** |
| **CO4** | **Understands control methods and fixes** |
| **CO5** | **Design EMC and interconnection** |

**Course Content:**

| **Unit-1** | **Basic Concepts** | **8 hours** |
|---|---|---|
| History and concept of EMI, Definition of EMI and EMC with examples, Classification of EMI/EMC, Units of Parameters, Sources of EMI, EMI coupling modes, ESD Phenomena and effects, Transient phenomena and suppression, Electro magnetic environment, Practical experiences and concerns, frequency spectrum conservations, mechanisms of EMI generation, EMI testing, Methods of elimination of EMI | | |
| **Unit-2** | **EMI Measurements** | **8 hours** |
| Basic principles of RE, CE, RS and CS measurements, EMI measuring instruments- Antennas, LISN, Feed through capacitor, current probe, EMC analyzer and detection technique open area site, shielded anechoic chamber, TEM cell, Natural and manmade sources of EMI/EMC: Sources of Electromagnetic noise, typical noise paths, modes of noise coupling, designing for EM compatibility, lightening discharge, electro static discharge (ESD), electro magnetic pulse (EMP). | | |
| **Unit-3** | **EMC Standard and Regulations** | **8 hours** |
| National and International standardizing organizations- FCC, CISPR, ANSI, DOD, IEC, CENEEC, FCC CE and RE standards, CISPR, CE and RE Standards, IEC/EN, CS standards, Frequency assignment - spectrum conversation, Components for EMC and EMC Standards: Choice of capacitors, inductors, transformers and resistors. | | |
| **Unit-4** | **EMI Control Methods and Fixes** | **8 hours** |
| Grounding, Bonding, Filtering, EMI gasket, Isolation transformer, opto isolator, Shielding and Bonding: effectiveness of shielding, near and far fields / impedances, methods of analysis, total loss due to absorption and reflection effects, composite absorption and reflection losses for electric fields / magnetic fields, magnetic materials as a shield, shield discontinuities, slots and holes, seams and joints, conductive gaskets, Electrical Bonding, Shape and Material for Bond straps. | | |
| **Unit-5** | **EMC Design and Interconnection Techniques** | **8 hours** |
| Cable routing and connection, Component selection and mounting, PCB design- Trace routing, Impedance control, decoupling, Zoning and grounding, Grounding and Cabling: Safety and signal grounds, low and high frequency grounding methods, grounding of amplifiers and cable shields, isolation, neutralizing transformers, shield grounding at high frequencies, digital grounding, types of cables, mechanism of EMI emission / coupling in cables | | |

**Continuous Assessment Pattern**

| Internal Assessment (IA) | Mid Term Test (MTE) | End Term Test (ETE) | Total Marks |
|---|---|---|---|
| 20 | 30 | 50 | 100 |

| Name of The Course | DSP Architecture | | | |
|---|---|---|---|---|
| Course Code | | | | |
| Prerequisite | | | | |
| | L | T | P | C |
| | 3 | 0 | 0 | 3 |

**Course Objectives:**.

Identify and formalize architectural level characterization of P-DSP hardware

Ability to design, programming (assembly and C), and testing code using Code Composer

Studio environment

Deployment of DSP hardware for Control, Audio and Video Signal processing

applications

Understanding of major areas and challenges in DSP based embedded systems

**Course Outcomes**

| | |
|---|---|
| **CO1** | Understand the hardware and software structures used to implement digital signal processing. |
| **CO2** | Describe the details of Architectures For Programmable DSP Devices. |
| **CO3** | Describe Programmable Digital Signal Processors TMS320C54XX addressing modes, control unit and its operation. |
| **CO4** | Implement basic DSP algorithms like FIR and IIR digtal filters. |
| **CO5** | Describe interfacing of memory and input output peripherals to programmable DSP devices |

**Text Book (s)**

1. B Venkataramani and M Bhaskar “Digital Signal Processors”, TMH, 2002.

2. Peter Pirsch “Architectures for Digital Signal Processing”, John Weily, 2007.

3. Avatar Singh and S. Srinivasan, “Digital Signal Processing”, Thomson Learning, 2004

**Reference Book (s)**

1. Lars Wanhammer, “DSP Integrated Circuits”, 1999 Academic press, New York

2.A.V.Oppenheim et.al, “Discrete-time Signal Processing”, Pearson Education, 2000.

3. Emmanuel C. Ifeachor, Barrie W. Jervis, “Digital signal processing – A practical approach”, Second Edition, Pearson Education, Asia.

4.Keshab K.Parhi, “VLSI Digital Signal Processing Systems design and Implementation”, John Wiley & Sons, 1999.

**Course Content:**

| Unit-1 | Introduction to Digital Signal Processing | 8 hours |
|---|---|---|
| Introduction, A Digital Signal-Processing System, The Sampling Process, Discrete Time Sequences, Typical DSP Algorithms (Discrete Fourier Transform (DFT) and Fast Fourier Transform (FFT), Least Mean Square(LMS) ). Representation of Signal Processing Algorithms, Signal-Flow, Data-Flow graphs, Digital Filters, Decimation and Interpolation, Analysis and Design Tool for DSP Systems. | | |
| **Unit-2** | **Architectures For Programmable DSP Devices** | **8 hours** |

| | | |
|---|---|---|
| Basic Architectural features, DSP Computational Building Blocks, Bus Architecture and Memory, Data Addressing Capabilities, Address Generation Unit, Programmability and Program Execution, Speed Issues, Features for External interfacing. | | |
| **Unit-3** | **Programmable Digital Signal Processors** | **8 hours** |
| Commercial Digital signal-processing Devices, Data Addressing modes of TMS320C54XX DSPs,Data Addressing modes of TMS320C54XX Processors, Memory space of TMS320C54XX Processors, Program Control, TMS320C54XX instructions and Programming, On-Chip peripherals, Interrupts of TMS320C54XX processors, Pipeline Operation of TMS320C54XX Processors. | | |
| **Unit-4** | **Implementation Of Basic DSP Algorithms** | **8 hours** |
| The Q-notation, FIR Filters, IIR Filters, interpolation Filters, Decimation filters, PID Controller, Adaptive Filters. Implementation of FFT algorithms. | | |
| **Unit-5** | **Interfacing Memory And I/O Peripherals To Programmable Dsp Devices** | **8 hours** |
| Memory space organization, External bus interfacing signals, Memory interface, Parallel I/O interface, Programmed I/O, Interrupts and I/O, Direct memory access (DMA). A Multichannel buffered serial port (McBSP), McBSP Programming, a CODEC interface circuit, CODEC programming, A CODEC-DSP interface example. | | |

**Continuous Assessment Pattern**

| **Internal Assessment (IA)** | **Mid Term Test (MTE)** | **End Term Test (ETE)** | **Total Marks** |
|---|---|---|---|
| 20 | 30 | 50 | 100 |

| Name of The Course | MIXED SIGNAL IC DESIGN | | | |
|---|---|---|---|---|
| Course Code | MVLS6008 | | | |
| Prerequisite | | | | |
| | L | T | P | C |
| | 3 | 0 | 0 | 3 |

**Course Objectives:**.

Understand basics of Data Converters and describes the concepts of modulator, filters to improve SN and SPICE modeling

**Course Outcomes**

| | |
|---|---|
| **CO1** | Understand basic concept of ADC, DAC |
| **CO2** | Learn SNR improvement methods |
| **CO3** | Know noise shaping data converters |
| **CO4** | Design data converters |
| **CO5** | Design various filters |

**Text Book (s)**


1. R. J. Baker, CMOS Mixed Signal Cicuit Design, Wiley/IEEE, 2002.
2. Handkiewicz, Mixed-Signal Systems : A Guide to CMOS Circuit Design, Wiley-IEEE, 2002.
3. Razavi, Principles of Data Conversion System Design, IEEE Press, 1995


**Reference Book (s)**


1. E. Sanchez-Sinencio and A. G. Andreou, Low-Voltage/Low-Power Integrated Circuits and Systems: Low-Voltage Mixed-Signal Circuits, IEEE, 1999.
2. Y. Tsividis, Mixed Analog-Digital VLSI Devices and Technology, MH, 1996.
3. S. Rabii and B. A. Wooley, Design of Low-Voltage Low-Power Sigma-Delta Modulators, Kluwer, 1998.
4. P. G. A. Jespers, Integrated Converters : D-A and A-D Architectures, Analysis and
5. Simulation, OUP, 2001.
6. R. Van de Plassche, Integrated Analog-to-Digital and Digital-to-Analog Converters Kluwer, 1994.


**Course Content:**

| Unit-1 | Data Converters | 8 hours |
|---|---|---|
| Data Converters: Introduction, Characteristic Parameters, Basic DAC and ADC Architectures. Sampling and Aliasing, SPICE models for DACs and ADCs, Quantization Noise. | | |
| **Unit-2** | **Data Converters SNR** | **8 hours** |
| Clock Jitter, Improving SNR using Averaging, decimating filters for ADC's, Interpolating filters for DAC's, Band pass and high pass Sinc filters, using feedback to improve SNR. | | |
| **Unit-3** | **Noise Shaping Data Converters** | **8 hours** |
| Noise Shaping data converters: SPICE model, First order noise shaping, First order Noise Shaping, - Digital first order NS Modulators, Modulation Noise, Decimating and filtering the output of a NS Modulator, Analog Sync filter using SPICE, Analog Implementation of First order NS Modulator, Feedback DAC, Forward modulator, op-amp. Second order Noise Shaping. | | |

| | | |
|---|---|---|
| **Unit-4** | **Implementing Data Converters** | **8 hours** |
| Implementing data converters: R-2R topologies for DAC's – Current mode, voltage mode, wide swing current mode DAC, topologies without an op-amp, effects of op-amp parameters. Implementing ADC's- Implementing S/H,Cyclic ADC, Pipeline ADC using1.5 bits per stage, capacitor error averaging, comparator placement, clock generation, offsets and alternative topologies, Layout of Pipelined ADC's. | | |
| **Unit-5** | **Filters** | **8 hours** |
| Low Pass filters, active RC integrators, Effect of parameters of Integrator, MOSFET-C integrators, transconductance-C integrator, discrete time integrators. Filtering topologies - bilinear transfer function and biquadratic transfer function | | |

**Continuous Assessment Pattern**

| **Internal Assessment (IA)** | **Mid Term Test (MTE)** | **End Term Test (ETE)** | **Total Marks** |
|---|---|---|---|
| 20 | 30 | 50 | 100 |

| Name of The Course | RESEARCH SEMINAR | | | |
|---|---|---|---|---|
| Course Code | MVLS9997 | | | |
| Prerequisite | | | | |
| | L | T | P | C |
| | 0 | 0 | 2 | 1 |

**Course Objectives:**.

1. To make literature survey for various recently emerging technologies.

2. To select any topic of interest and to review the related literature in detail.

3. To compare and analysis the various topologies for the selected topic of interest.

4. To conclude the advantage, drawbacks and future scope of the technique.

**Course Outcomes**

| | |
|---|---|
| **CO1** | Get familiar with the recently advanced techniques. |
| **CO2** | Get detailed information about the topic of interest. |
| **CO3** | Know how to do literature survey. |
| **CO4** | Develop the interest in research in area of VLSI Design |

**Text Book (s)**

Depending upon the area of interest student may choose any text book of relevant field

**Continuous Assessment Pattern**

| Internal Assessment (IA) | End Term Test (ETE)(Presentaion) | Total Marks |
|---|---|---|
| 50 | 50 | 100 |