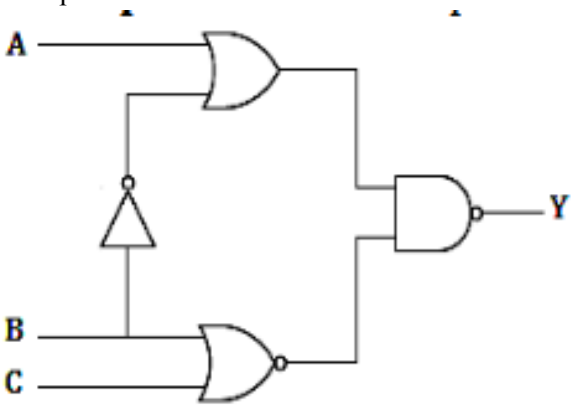
Name. _____ **Student Admn. No.: _____**	**Printed Pages:01**

School of basic Science
Summer Term Examination – July - August 2024
[Programme: B.Sc **] [Semester: VI) [Batch: All]**

Course Title: Analog and Digital Principles and Applications **Course Code: C1UD604B**	**Max Marks: 100** **Time: 3 Hrs.**

Instructions:
1. *All questions are compulsory.*
2. *Assume missing data suitably, if any.*

		K Level	COs	Marks
	SECTION-A (15 Marks) **5 Marks each**			
1.	Discuss the construction and working of JFET.	KL1	CO2	5
2.	a) What is 2's complement of the number 1101101? b) Add -5 and -4 using 2's complement.	KL1	CO3	5
3.	Find the expression for output 	KL2	CO4	5
	SECTION-B (40 Marks) **10 Marks each**			
4.	What do u mean by universal gate? Draw the NAND gate using transistors and write the truth table	KL3	CO4	10
5.	Design a Full – Adder using two Half - Adder and OR gate, draw the Block diagram with logic circuit?	KL3	CO4	10
6.	Define built-in-potential (potential barrier). What will be direction of internal electric field developed due to potential barrier in a zero biased p-n junction diode?	KL4	CO1	10
7.	Using two port network, draw the h parameters for common base configuration and calculate the gain.	KL4	CO2	10
	SECTION-C (45 Marks) **15 Marks each**			
8.	Explain the truth table of half subtractor and design the half subtractor circuit using NOR gates?	KL5	CO4	15
9.	Estimate the resistance of an intrinsic Ge rod 1 mm long, 1 mm wide and 1 mm thick at 300 K. the intrinsic carrier density $2.5 \times 10^{19}\ m^{-3}$ is at 300 K and the mobility of electron and hole are 0.39 and 0.19 $m^2\ v^{-1}\ s^{-1}$.	KL5	CO1	15
10	In SR flip flop describe the (a) circuit diagram using NAND gates; (b) truth table; (c) logic symbol; (d) find out the Boolean equation using K-map.	KL5	CO4	15