GALGOTIAS UNIVERSITY

ADMISSION NUMBER

School of Engineering

B.TECH Electronics and Communication Engineering
Summer / Backlog - Semester End Examination - Jul /Aug 2024

Duration : 180 Minutes
Max Marks : 100

Sem III - G2UC301C / BECE2015 - Electronic Devices and Circuits

General Instructions
Answer to the specific question asked
Draw neat, labelled diagrams wherever necessary
Approved data hand books are allowed subject to verification by the Invigilator

1)	Write about formation of unbiased PN junction diode.	K1(2)
2)	Explain the operation of forward biased and reverse biased PN junction Diode.	K2(4)
3)	Explain the working of NPN and PNP transistor.	K2(6)
4)	Define cutoff and active region of a transistor.	K3(9)
5)	Draw and explain the input/output characteristics of a transistor in CE configuration	K3(9)
6)	Define the current ICEO for an transiostor circuit.	K5(10)
7)	What are the features of JFET?	K4(12)
8)	Why is emitter follower so named?	K5(15)
9)	Explain single and double tuned amplifier, Compare Single Tuned and Double Tuned Amplifier in terms of examples.	K5(15)
10)	Draw the circuit diagram of a current series feedback amplifier and derive expressions for voltage gain with and without feedback.	K6(18)