GALGOTIAS UNIVERSITY

ADMISSION NUMBER												

School of Computing Science and Engineering

Bachelor of Technology in Computer Science and Engineering
Summer Term Examination – July - August 2024

Duration : 180 Minutes
Max Marks : 100

Sem V - E2UC505T - Computer Organisation and Architecture

General Instructions
Answer to the specific question asked
Draw neat, labelled diagrams wherever necessary
Approved data hand books are allowed subject to verification by the Invigilator

1)	Express the given conditional control statement using two register transfer statements accompanied by their corresponding control functions. If (A=1) then (R5 <--- R7) else If (B=1) then (R5 <--- R6)	K1	(2)
2)	Discuss differences between SRAM and DRAM.	K2	(4)
3)	Convert the following arithmetic expressions from infix to reverse Polish notation (3 * 4) + (5 * 6) Also show scack operations to evaluate (3 * 4) + (5 * 6)	K2	(6)
4)	A computer is designed for 32-bit instructions and 12-bit addresses. If there are 250 two-address instructions then calculate the maximum number of one-address instructions that can be generated?	K3	(9)
5)	With the help of diagram, describe connection of I/O bus and I/O devices.	K3	(9)
6)	Explain programmed I/O and interrupt-initiated I/O in detail with the help of diagram.	K5	(10)
7)	Explain Daisy-Chaining priority and Parallel priority Interrupt with its hardware diagram.	K4	(12)
8)	Convert the following arithmetic expressions from reverse Polish notation to infix notation. (a) A B C D E + * - / (b) A B C D E * / - + (c) A B C * / D - E F / + (d) A B C D E F G + * + * + *	K5	(15)
9)	Explain page replacement with the help of figure. Discuss FIFO algorithm for page replacement. Main memory has 3 page frames (frame 0, frame 1 and frame 2). Pages from virtual memory are required in the order 2,3,2,1,5,2,4,5,3,2,5,2 . Calculate hit ratio using (1) FIFO Algorithm	K5	(15)

10) The outputs of four registers, R0, R1, R2 and R3, are connected through 4X1 multiplexers to the inputs of a fifth register, R5. Size of each register is of 8 bit. The specified transfers are determined by four timing variables P0 through P3 as given below. K6 (18)

P0: R5<---R0
P1: R5<---R1
P2: R5<---R2
P3: R5<---R3

The timing variables are mutually exclusive, signifying that only one variable equals 1 at any given time, with the other three set to 0. Illustrate a block diagram that displays the hardware implementation of the register transfers. Include the essential connections from the four timing variables to the selection inputs of the multiplexers and to the load input of the register R5.