GALGOTIAS UNIVERSITY

ADMISSION NUMBER

School of Computing Science and Engineering

Bachelor of Technology in Computer Science and Engineering
Summer Term Examination – July - August 2024

Duration : 180 Minutes
Max Marks : 100

Sem III - E2UC301T - Computer Organisation and Architecture

General Instructions
Answer to the specific question asked
Draw neat, labelled diagrams wherever necessary
Approved data hand books are allowed subject to verification by the Invigilator

1)	Explain parallel processing.	K1(2)
2)	Explain why each of the following micro operation can not be executed during a single clock pulse in the system of basic computer register connected to a common bus. Specify a sequence of micro operations that will perform the operation. (i)IR<- M[PC] (ii) AC<-AC + TR (iii) DR<-DR + AC	K2(4)
3)	Design the following combinational circuit of 4-bit Decrementer using 4-bit parallel adder.	K2(6)
4)	Outline the various parts of a magnetic disk, and relate the following term w.r.t. disk in a formulae. access time, seek time,rotational delay, transfer time.	K3(9)
5)	Design a 4- bit full adder using two half adders.	K3(9)
6)	A bus organized CPU based on general register organization has 16 registers with 32 bits in each , an ALU, and a destination decoder. (i) How many multiplexers are there in the A bus, and what is the size of each multiplexer. (ii) How many selection inputs are needed for MUX A and MUX B? (iii) How many inputs and outputs are there in the decoder? (iv) How many inputs and outputs are in the ALU for data, including input and output carries? (v) Formulate a control word for the system assuming that the ALU has 65 operations.	K5(10)
7)	Draw a common bus system for a digital computer system having 4 registers and each registers of 4-bit. Instead of multiplexers, you have to use three state-buffers and a decoder to design this bus.	K4(12)
8)	With the help of timing diagrams and sequence of events, justify Source initiated and Destination initiated transfer using hand shaking is better than Source initiated and Destination initiated transfer using strobe control Technique.	K5(15)
9)	Show the contents of registers E, A, Q and SC during the process of multiplication of two binary numbers 11111 (multiplicand) and 10101 (multiplier). The signs are not included.	K5(15)
10)	Design a 4-bit arithmetic circuit that can perform addition, subtraction, increment and decrement micro-operations.	K6(18)