GALGOTIAS UNIVERSITY

ADMISSION NUMBER												

School of Engineering

B.TECH Electronics and Communication Engineering in Artificial Intelligence and Machine
Semester End Examination - Jun 2024

Duration : 180 Minutes
Max Marks : 100

Sem IV - G2UA401B - Integrated Circuits

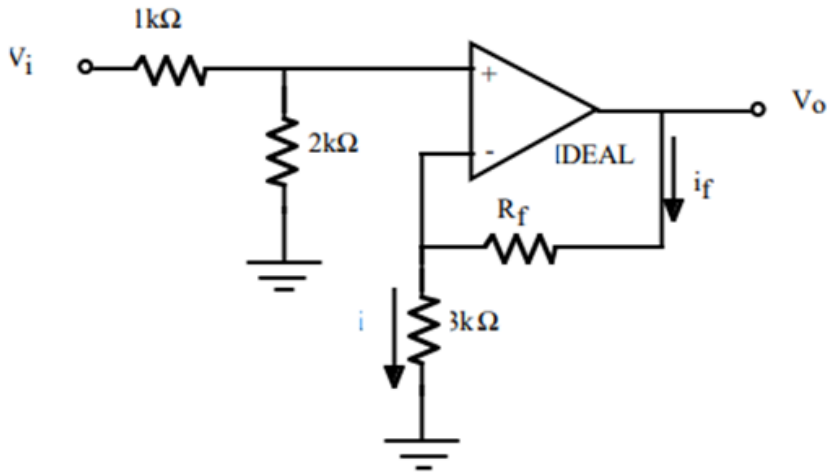
General Instructions
Answer to the specific question asked
Draw neat, labelled diagrams wherever necessary
Approved data hand books are allowed subject to verification by the Invigilator

1) List the application of PLL. K1 (2)

2) Explain Why open loop op-amp configurations are not used in linear applications? K2 (4)

3) How the multiplier IC used as the frequency doubler? K2 (6)

4) For the ideal op amp shown below, what should be the value of resistor Rf to obtain a gain of 5? K3 (9)



5) Define resolution and Calculate the resolution of an 8-bit DAC. K3 (9)

6) What criteria should be kept in mind while selecting any DAC. K5 (10)

7) Analyse and explain the block diagram of Opto-electronic-integrated circuit(OEIC). K4 (12)

8) Determine the working of square wave generator. K5 (15)

9) Elaborate the pin diagram of 555 timer IC. K5 (15)

10) The slew rate of an op-amp is 0.5 V/μS when used as an inverting amplifier with a gain of 50. The voltage gain vs frequency curve is flat upto 20 kHz. Find out the maximum peak to peak input signal can be applied without distorting the output. K6 (18)