GALGOTIAS UNIVERSITY

ADMISSION NUMBER

School of Computing Science and Engineering

Bachelor of Technology in Computer Science and Engineering
Semester End Examination - Jun 2024

Duration : 180 Minutes
Max Marks : 100

Sem VI - R1UC619T - Advanced Computer Architecture

General Instructions
Answer to the specific question asked
Draw neat, labelled diagrams wherever necessary
Approved data hand books are allowed subject to verification by the Invigilator

1)	Pointout the way for Prediction to reduce Hit Time.	K1(2)
2)	Explain the role of SIMD extensions in accelerating multimedia applications.	K2(4)
3)	With a neat diagram explain the classic five stage pipeline for a RISC processor.	K2(6)
4)	Demonstrate the Cache Coherence Performance issues.	K3(9)
5)	You are tasked with designing a systolic array for accelerating the computation of a large matrix multiplication operation. The matrix dimensions are 1000x1000, and the systolic array has 16 processing elements arranged in a 4x4 grid. Calculate the total number of clock cycles required to complete the matrix multiplication operation, assuming each processing element can compute one multiply-accumulate operation per clock cycle.	K3(9)
6)	Comment on the performance impact of SIMD optimizations across different multimedia workloads, considering factors such as data parallelism, instruction-level parallelism, and memory bandwidth utilization.	K5(10)
7)	Examine how Pipelined Cache Access used to Increase Cache Bandwidth.	K4(12)
8)	Provide various mechanisms to handle dependencies.	K5(15)
9)	Critically assess the transformative nature of cloud computing as a paradigm for facilitating convenient, on-demand network access to a shared pool of configurable computing resources.	K5(15)
10)	State two performance equations of CPU. Derive an expression for CPU clock as a function of instruction count, clocks per instruction and clock cycle time.	K6(18)