GALGOTIAS UNIVERSITY

ADMISSION NUMBER												

School of Computing Science and Engineering

Bachelor of Technology in Computer Science and Engineering
Mid Term Examination - Nov 2023

Duration : 90 Minutes
Max Marks : 50

Sem V - E2UC505T - Computer Organisation and Architecture

General Instructions
Answer to the specific question asked
Draw neat, labelled diagrams wherever necessary
Approved data hand books are allowed subject to verification by the Invigilator

1)	To make common bus for 8 register of 16 bit each, evaluate how many multiplexers are needed and what will be size of each multiplexer.	K1	(1)
2)	Perform the logic AND, OR and XOR micro operation with the two binary strings 100111100 and 10101010.	K2	(2)
3)	The provided transfer statements define a memory operation. Describe the memory operation for each statement. (a) R7<---M [AR] (b) M [AR} <---R8 (c) R9 <---M [R9]	K3	(3)
4)	In a gereral register organization comprising a multiplexer, ALU, decoder, and register, the following propagation delays are specified: (i) 40 ns for signals to propagate through the multiplexer (ii) 90 ns to execute the ADD operation in the ALU (iii) 30 ns delay in the destination decoder (iv) 20 ns to clock the data into the destination register. Calculate the minimum cycle time achievable for the clock? Justify the answer after drawing the block diagram of gereral register organization.	K3	(6)
5)	Convert the following numerical arithmetic expression into reverse Polish notation and show the stack operations for evaluating the numerical result. (3 + 4)[10(2 + 6) + 8]	K3	(9)
6)	Use Booth algorithm to multiply 10010 X10100.	K4	(8)
7)	Explain the funtion of parallel adder. Make the block diagram for the hardware that implements the following statements: w +yz : AR <---- AR + BR For this hardware implementation, AR and BR are n-bit registers and w, y, and z are control variables. Also, make hardware for the control function.	K5	(15)
8)	Construct the hardware that executes following statement. This should involve illustrating the logic gates for the control function, as well as providing a block diagram for the binary counter incorporating a count enable input. abP0 + P1 + b P2 : AR <---AR + 1	K6	(6)