School of Electrical Electronics and Communication Engineering

Electronics and Communication Engineering

ETE - Jun 2023

Time : 3 Hours **Marks : 50**

Sem VI - BECE3013 - VLSI Design

Your answer should be specific to the question asked

Draw neat labeled diagrams wherever necessary

1.	List the disadvantages of scaling a MOSFET	K1 CO2	(2)
2.	List the three major elements of power dissipation in CMOS Circuits.	K2 CO3	(2)
3.	Draw the CMOS logic structure of AND logic	K2 CO4	(2)
4.	Compare front end and back end design flows of VLSI	K2 CO5	(2)
5.	List out the benefits of Epitaxial Growth.	K1 CO1	(2)
6.	Write short notes on Standard Cell Libraries. How Standard cell libraries can be classified based on density and threshold voltage?	K4 CO6	(6)
7.	Comment on Photoresists. Explain its types	K3 CO2	(5)
8.	How non-volatile solid film on the substrate can be formed by the reaction of vapour phase chemicals? Explain	K3 CO1	(5)
9.	Explicate the Voltage Transfer Characteristics of a CMOS Inverter for different values of input voltages.	K4 CO3	(8)
10.	Write detailed notes on VLSI Design Flow.	K5 CO5	(8)
11.	Brief with necessary sketches (i) CMOS Transmission Gate (ii) Dynamic CMOS Design	K5 CO4	(8)